Testing CMOS Digital ICs with Analog Techniques

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Abstract. In this thesis three novel analog techniques for testing CMOS Integrated circuits are presented. These techniques are based on analog circuits since they offer a number of important advantages compared to standard digital test techniques, such us less silicon area, lower power consumption and high operating speed. Therefore, the proposed techniques can be embedded in the circuit under test, contributing to the design of more reliable circuits.

Keywords: Self Checking Checkers, Two Rail Code Checkers, Current Mode Checker, Periodic Output Checkers. Soft Errors, Sense Amplifier, Timing Errors, I_{DDQ} testing, Current Mirror Amplifier

1 Introduction

A widely used error detection code in fault secure systems is the Two Rail Code (TRC) [3]. The first analogue technique of this thesis is a current mode, parallel TRC checker suitable for the implementation of high fan-in embedded checkers. The new circuit belongs to the periodic outputs category of TRC checkers and provides high testability since it is totally self-checking (TSC) [1] or strongly code-disjoint (SCD) [2] for a wide set of realistic faults, including transistor stuck-open faults that are not covered by other TRC checkers in the same category. Any TSC checker is capable to detect all internal faults if all codewords are available at the checkers' inputs. Designs of the proposed TRC checker, in a standard $0.18\mu m$ CMOS technology proved the efficiency of the circuit over earlier topologies in the same category, in terms of silicon area requirements, speed performance and power consumption.

A very important class of faults is the transient faults that cause soft or timing errors due to a variety of mechanisms, such as radiation, power supply noise, e.t.c. The shrinking of dimensions in CMOS technology makes digital circuits more sensitive to such mechanisms. We propose a novel and fast concurrent soft and timing error detection circuit for CMOS ICs based on current mode sense amplifier topologies. The circuit exploits the temporary nature of the transient faults as well as the delayed response of the delay faults to detect the corresponding errors.

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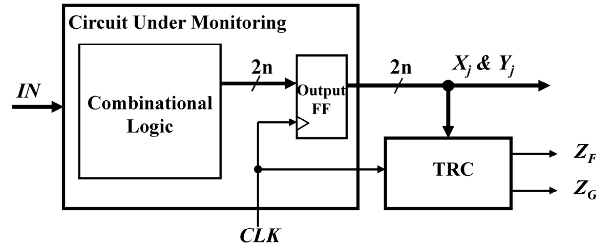

Fig. 1. A self-checking circuit with a TRC checker

Our third analogue fault detection technique is an I_{DDQ} testing technique. I_{DDQ} testing is a valuable manufacturing tool to achieve high defect detection levels and improve quality and reliability of CMOS ICs. A new I_{DDQ} testing technique, a suitable embedded circuit to support it and a theoretical model for the circuit operation are presented in this thesis. In deep submicron technologies, the discrimination between defective and non-defective I_{DDQ} currents is hard. In order to be able to exploit I_{DDQ} testing in nanometer technologies we propose a new I_{DDQ} testing approach where the background current at the sensing node is properly controlled taking into account possible process and temperature variations as well as the dependence of the background current on the applied test vector. The adoption of this method is a promising way to extend the viability of I_{DDQ} testing in the nanometer technologies.

This abstract is organized as follows. In Section 2 the proposed TRC checker is presented along with a modified version for enhanced testability. In Section 3 a new circuit for soft and timing error detection based on a sense amplifier is given and finally in Section 4 the proposed technique for I_{DDQ} testing is presented.

2 A Current Mode, Parallel Two-Rail Code Checker

A new parallel, fast and low silicon area cost TRC checker is proposed in this thesis. The new checker has periodic outputs (in each clock semi-period they have alternating complementary values) and it is based on the current mode structure we introduced in [6]. It is suitable for the implementation of embedded, high fan-in TRC checkers. The new checker is proved to be TSC or SCD for a wide set of realistic faults, while a modified version of it covers transistor stuck-open faults that are not fully detectable in earlier TRC checker designs [5]. Note that stuck-open faults present a considerable interest in very deep submicron technologies [7, 9]. In addition, like in [5], the checker requires only two input codewords, out of a wide variety of equivalent pairs, to satisfy the TSC or SCD property for the enhanced set of faults.

The general topology of a circuit that is monitored by a two-rail code (TRC) checker is shown in Fig. 1. The circuit under monitoring is designed to produce two-railed output words ($X_j, Y_j,\ j \in\ [1, \ldots, n]$) when it is fault-free ($X_j = \overline{Y}_j$) and non two-railed output words ($X_j = Y_j$) in case of internal faults.

The proposed n-variable TRC checker is presented in Fig. 2. The circuit is divided into two identical sub-blocks, the F-SubBlock (FSB) and the G-SubBlock (GSB); it receives n pairs of two-railed inputs $(X_j, Y_j, j \in [1, \ldots, n])$ and provides a two-railed pair of outputs Z_F and Z_G, one for each sub-block. Since this checker belongs to the periodic outputs TRC checkers category, it has been designed so that the outputs Z_F and Z_G present alternating complementary logic values in each semi-period of the clock signal. The first sub-block is fed by half of the checker input pairs $(X_r, Y_r, r \in [1, \ldots, k]$, where $k = n/2)$ and the complementary clock signal $CLKB$ while the second is fed by the rest of the input pairs $(X_s, Y_s, s \in [k+1, k+2, \ldots, n])$ and the clock signal CLK.

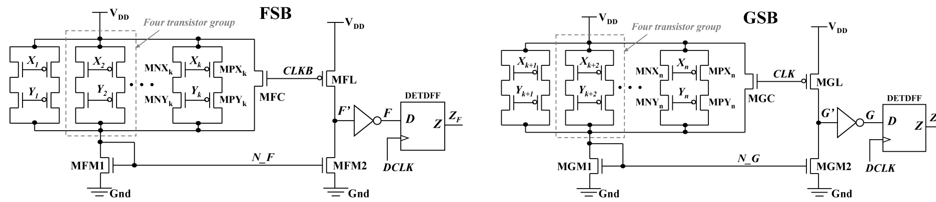

Fig. 2. The proposed two-rail code checker, $k = n/2$

The checker's outputs Z_F and Z_G always present complementary logic values in the fault free operation of the circuit under monitoring and non-complementary in the opposite case. The checker operation is described in [10] and is transparent to the circuit under monitoring.

The waveforms in Fig. 3 show the response of the checker's nodes F and G in the presence of codeword inputs and all possible non-codeword input conditions. In all three cases, the Z_F and Z_G outputs of the checker will capture the responses on F and G indicating the presence of errors or not and the proposed circuit is proved to be code-disjoint.

It is proved [11] that the proposed checker is TSC for the following kind of faults: line stuck-at faults, Transistor Stuck-On (TSON) faults, transient faults, Transistor Stuck Open (TSOP) faults (except for the 4 input transistors) and finally bridging faults. The proposed parallel TRC checker has been designed in the standard $0.18\mu m$ CMOS technology of ST Microelectronics for a variety of n-variable values (number of inputs) ranging from 8 to 512 and the operation has been verified by electrical simulations in a full range of PVT (Process, Voltage, Temperature) conditions, that is: a) the process corners for the used technology provided by ST, b) power supply variations up to 10% and c) temperature variations from 0^oC to 125^oC. In Table 1 design issues and simulation results are presented for the proposed checker and the checker presented in [5].

According to Table 1, the proposed in this work checker is superior over the checker in [5] with respect to the required silicon area and the response delay time, especially for high values of the n-variable.

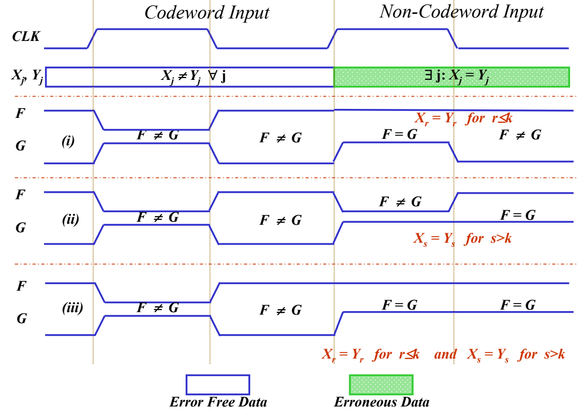

Fig. 3. Checker's response under codeword and non-codeword inputs

Table 1. Comparisons with respect to i) silicon area, ii) response delay time and iii) power consumption

Fan-in	Silicon Area Cost (UST)			Response Delay (ps)			Power Consumption (μW)		
-n-	Proposed	[5]	Reduction	Proposed	[5]	Reduction	Proposed	[5]	Reduction
8	187	252	25.8%	298	355	16.1%	64	21.3	-200.5%
16	239	415	42.4%	328	505	35.0%	95	27.7	-243,0%
32	342	776	55.9%	375	775	51.6%	109	40	-172.5%
64	540	2324	76.8%	408	1205	66.1%	119	87.1	-36.6%
128	924	7925	88.3%	517	1845	72.0%	136	245	44.5%
256	1663	34965	95.2%	695	3097	77.6%	174	976	82.2%
512	3106	135675	97.7%	1055	4965	78.8%	215	3840	94.4%

In order to extend the self-checking property of the circuit to the uncovered TSOP faults a modified version is presented in Fig. 4. In the new circuit there is a fifth nMOS transistor in the group of the four transistors (Fig. 2) that is controlled by a select signal S_j. The select signals S_j ($j \in [1, \ldots, n]$) are generated by a Cyclic Shift Register (CSR) of $k = n/2$ bits and a NOR gate array [11]. The S_j signals get successively one after the other the value "1" and thus test for TSOP the four transistors of the group including the fifth transistor that is driven by the signal S_j. It is proved [11] that the modified checker satisfies the self-checking property with respect to the same set of faults as in its previous version including the TSOP faults for the input transistors, in case that this is imperative for the design [8, 9]. Note that the parallel TRC checker presented earlier in [5] does not provide a full coverage of the TSOP faults. The proposed checker needs the application of only two codewords to satisfy the TSC or SCD properties, similarly to the checkers in [4, 5]. This is a very important property for embedded checkers.

The modified version of the proposed parallel two-rail code checker has been also designed in the same $0.18\mu m$ CMOS technology ($V_{DD} = 1.8V$), for n-variable ranging from 8 to 512. The operation of the checker has been verified by electrical simulations in a full range of PVT conditions, for all possible con-

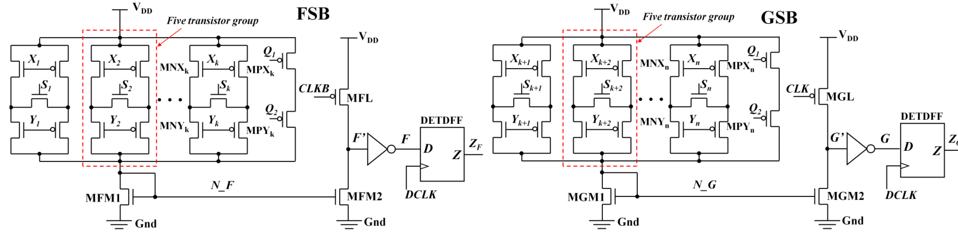

Fig. 4. The modified two-rail code checker, $k = n/2$

ditions. Monte Carlo mismatch analysis has been performed and the correct operation has been verified.

3 A Circuit for Concurrent detection of Soft and Timing errors in Digital CMOS ICs

The second analogue technique is a new soft and timing error detection circuit. It exploits the time redundancy approach that has been adopted in recent works [12, 13] and provides error tolerance in case that it will be combined with a retry cycle; that is, the correct result is obtained, each time an error is detected, by repeating the last operation using a lower frequency.

Fig. 5 presents a Functional Circuit consisting of the combinational part and the Flip-Flops of the output register. Transient faults on internal nodes of the combinational circuit may result in the appearance of transient pulses at its output lines OUT. In case that the triggering edge of the clock CLK arrives just after the transient pulse appearance and during its presence on the $OUT_{(a)}$ line (time interval δ), a soft error is generated at the output FFO of the Flip-Flop.

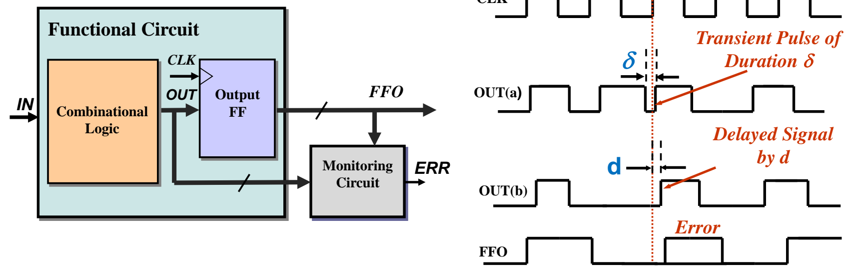

Fig. 5. Error generation mechanisms and error detection using a monitoring circuit

Moreover, path delay faults in the combinational circuit may result in a delayed signal arrival at a circuit output $OUT_{(b)}$, after the triggering edge of the

clock CLK (time interval d) and thus the generation of a timing error at the output FFO of the Flip-Flop. The key idea behind the adopted error detection technique is the use of a Monitoring Circuit to monitor the responses at the outputs of the Combinational Logic and the whole Functional Circuit after a time interval T from the latching edge of the clock signal CLK [12, 13].

In the fault free case no signal transitions appear on the monitored lines after the latching edge of the clock signal CLK and the error indication signal of the Monitoring Circuit (ERR) remains "low". In the case that a transient or a delay fault in the combinational logic causes a transient pulse or a delayed signal response (transition) on the output line OUT of the Combinational Circuit when the latter is sampled by the clock CLK, the Output Flip-Flop captures an erroneous value and an error occurs on its output FFO. The Monitoring Circuit detects the resulted difference between the values on the lines OUT and FFO and the error indication signal (ERR) rises to "high".

The proposed Monitoring Circuit that exploits a sense amplifier for soft and timing error detection is shown in Fig. 6 and consists of a Pre-Sensing Block (PSB), a Sense Amplifier (SA) and an Error Indication Flip-Flop (EIFF). The Pre-Sensing Block is divided into two sub-blocks (SBL and SBR) each one feeding a separate input of the sense amplifier INL and INR respectively.

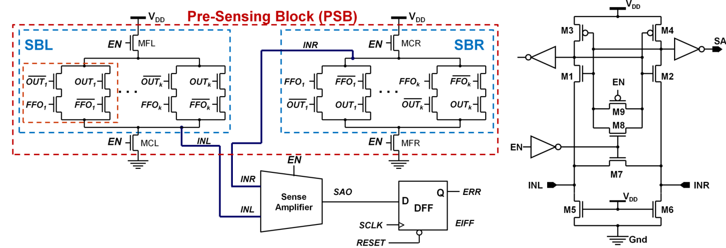

Fig. 6. The proposed Monitorting Circuit (left) and the Sense Amplifier (right)

The k pairs of monitored lines OUT_j and FFO_j ($j \in [1 \dots k]$), are driving both sub-blocks of the Pre-Sensing Block. The SA is activated by the EN signal and provides the output signal SAO, which is latched by the Error Indication Flip-Flop (EIFF). During the system operation each period of the clock CLK can be seen as divided in two phases, the normal phase and the monitoring phase, which are defined by the EN signal, as it is shown in Fig. 7. In the normal phase, the Monitoring Circuit is inactive (EN="low").

In the monitoring phase EN="high". In the error free case where $OUT_j = FFO_j (\forall j \in [1 \dots k])$ the SA will amplify the signal difference between its two inputs driving fast its output SAO to "low". In the presence of an error the SA will also amplify the signal difference between its inputs driving fast its output SAO to "high" providing the indication of error detection.

The $0.18\mu m$ CMOS technology of ST Microelectronics with $1.8V$ power supply has been exploited for the design of the proposed error Monitoring Circuit.

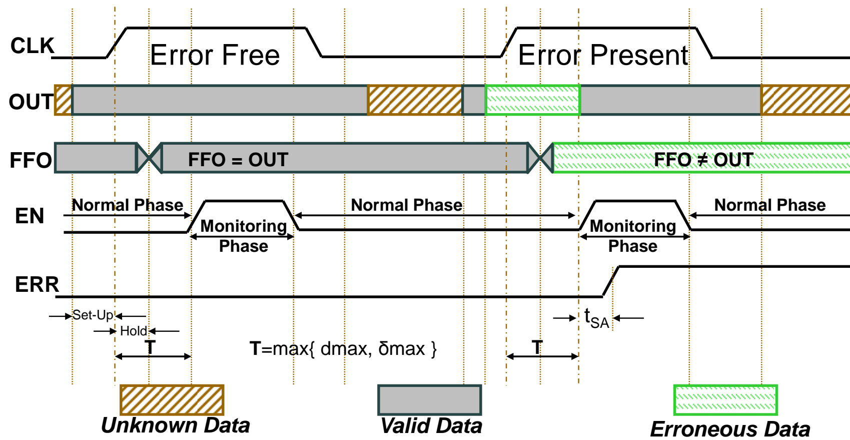

Fig. 7. Signals' timing for the Monitoring Circuit

The case of 72 monitored pairs and the corresponding layout design is given in Fig. 8. The "folded bit-line" design technique, is exploited in order to achieve a high density PSB and make the Monitoring Circuit insensitive to process and temperature variations.

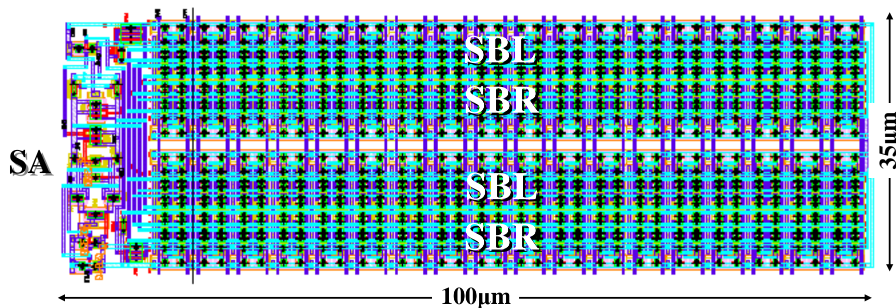

Fig. 8. Layout of the Monitoring Circuit for 72 monitored pairs of lines

Simulations and Monte Carlo analysis have been carried out [14, 15] for various numbers of monitored pairs (from 9 to 576), for temperatures up to 125^oC and using all process corner conditions. Table 2 presents comparisons between the detection times reported in [13] and the corresponding times in this circuit for various numbers of monitored pairs [16]. These measurements have been carried out at 125^oC and for the slow-slow transistor model, which, according to the simulations, provides the worst case response times.

Table 2. Detection time comparisons

Number of Monitored Pairs	Detection time (ps)		Reduction (%)
	[13]	Proposed	
9	456	191	58
18	501	226	55
36	581	265	54
72	721	317	56
144	979	376	62
288	1485	430	71
576	2480	468	81

4 Coping with current variations in I_{DDQ} testing

The quiescent current (I_{DDQ}) of a circuit is defined as the sum of its leakage currents (background current I_B), plus any defective current (I_{DEF}). I_{DDQ} monitoring is a well established technique for testing integrated circuits (ICs) in CMOS technologies. I_{DDQ} testing is based on the assumption that the intrinsic, defect-free, quiescent current of an IC is small compared to the quiescent current in the presence of a defect in the circuit. Consequently, setting the maximum current from the expected range of background currents in a circuit under test (CUT) as the threshold current, we can discriminate defect free from defective ICs by comparing their I_{DDQ} current with this threshold current.

Fig. 9 (left) presents an I_{DDQ} testing scheme based on the use of a Current Sensor (CS), either embedded to the IC (Built-In Current Sensor - BICS) or external to it. The Circuit Under Test (CUT) is isolated from the ground supply (*Gnd*) by MN_G transistor while the current sensor is connected to the virtual ground (*V_Gnd*) of the CUT. During the normal mode of operation the *V_Gnd* node is grounded. In the test mode of operation the signal T_ENB turns low and the CS compares the I_{DDQ} current of the CUT with a reference current (I_{REF}). In case that the I_{DDQ} current is greater than the I_{REF} current, the CUT is characterized as defective. According to the above scheme, the I_{REF} current must be greater than the maximum defect free background current I_B of the CUT.

In nanometer technologies the circuit background current I_B is increased with technology evolution [18]. Moreover, the defective current I_{DEF} that is required to be detectable is decreased [17]. In addition the number of transistors in a single chip is increased rapidly resulting in the reduction of the gap between the values of defect free and defective I_{DDQ} currents. Furthermore, the value of I_B is also influenced by temperature and increased process variations. Therefore, the application of I_{DDQ} testing using a unique reference current I_{REF} for discrimination between defect free and defective circuits for all chips in a production line, is impractical since it will either lead to yield loss or reduced fault coverage. Consequently, I_{REF} must be adjusted for each chip in order to take into account process variations.

The circuit in Fig. 9 (right) uses an extra transistor MN_T in parallel to MN_G, proper biased by voltage V_{bias} so that in the defect free case the volt-

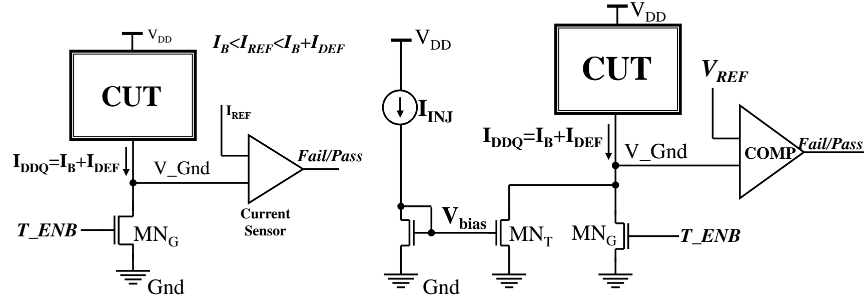

Fig. 9. A common I_{DDQ} testing scheme (left). The adjustable I_{DDQ} testing concept (right).

age at the virtual ground node (V_Gnd) is less than a reference voltage V_{REF}. The bias voltage V_{bias} can be generated using an injection current I_{INJ} and a current mirror. However, since the background current I_B of the CUT is influenced by process and temperature variations, the injection current I_{INJ} must be accordingly adjusted in order to avoid fault coverage reduction or yield loss.

In order to dynamically adjust I_{INJ} to process and temperature variations we adopted the partitioning of the CUT into two subcircuits (the left subcircuit sub-CUTL and the right subcircuit sub-CUTR). Then the background current of the left subcircuit is used as injection current (I_{INJ}) for the testing of the right subcircuit and vice-versa. Since in each case the background and the injection currents are influenced by the same process and temperature variations in the CUT, the I_{DDQ} testing process turns to be almost independent of these two factors.

In Fig. 10 the simplified block diagram of the proposed I_{DDQ} testing technique is presented, where the background current of sub-CUTL is used to generate the injection current for the I_{DDQ} testing of sub-CUTR. A preliminary study of this I_{DDQ} testing architecture and the built-in current sensing (BICS) circuit has been presented in [19] while early experimental results were discussed in [20] and [21].

The I_{DDQ} testing circuitry (consisting of the CMA, the comparator and transistors MN_{GL} and MN_{GR}) can be either embedded in the chip, forming a BICS circuit, or externally. Each partition must have a dedicated virtual ground (V_Gnd_L and V_Gnd_R respectively). In general the two subcircuits under consideration during I_{DDQ} testing are not identical. Consequently, their background currents I_{BL} and I_{BR} are not expected to be equal. In addition, the magnitude of each background current depends on the applied test vector. From the above it is evident that a tunable current mirror (a current mirror with tunable current gain β) is required in order to be able to generate for each test vector (j) the bias current $I_{B(L/R)j}$ from the injection current $I_{B(R/L)j}$ according to the following relation: $I_{B(L/R)j} = \beta_j I_{B(R/L)j}$. The proposed implemented tunable current mirror amplifier (T-CMA) is illustrated in Fig. 11.

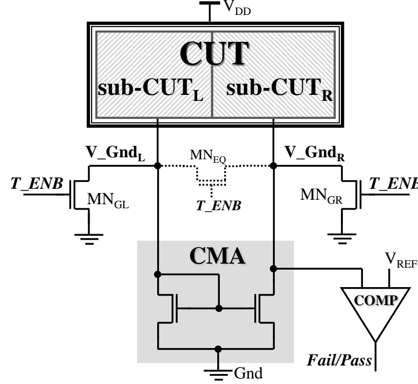

Fig. 10. The proposed I_{DDQ} testing technique

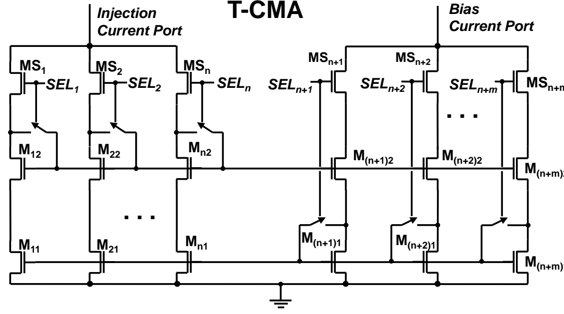

Fig. 11. A tunable current mirror amplifier (T-CMA)

In order to validate the proposed I_{DDQ} testing technique a demonstration circuit (consisting of a digital circuit and a BICS circuit) has been designed and fabricated (see Fig. 12) in a standard $180nm$ CMOS technology ($V_{DD} = 1.8V$). The digital circuit has been partitioned into two subcircuits. The microphotograph of the demonstrator is shown in Fig. 12.

Also in this Thesis a comprehensive theoretical analysis of the proposed technique is provided, in order to have a quantitative estimation of the trade-off between resolution (res), size of the partition of the CUT (N) and the size of the BICS.

The defective current resolution (res) is defined as the minimum amount of defective current that the BICS can distinguish to the total fault free background current of the CUT. In I_{DDQ} testing we want the resolution to be as small as possible so that small defective currents, or in other words high defective resistances (lighter defects), are detectable. From the analysis it is shown that as the circuit size is increased, a desired defective current resolution can be achieved by increasing the current mirror transistor widths. In Fig. 13 the defective current

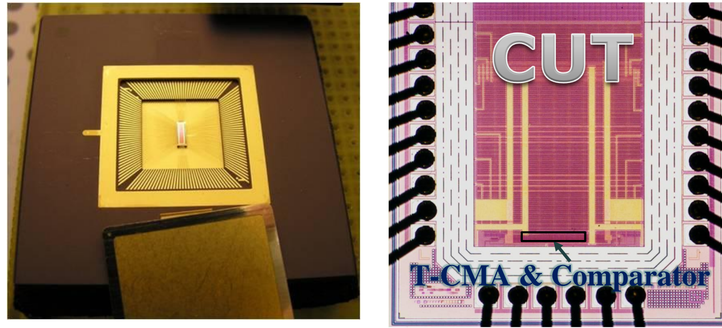

Fig. 12. Fabricated I_{DDQ} test chip and a microphotograph

resolution as a function of the transistor widths (W_R) in the current mirrors is presented for various circuit sizes (N).

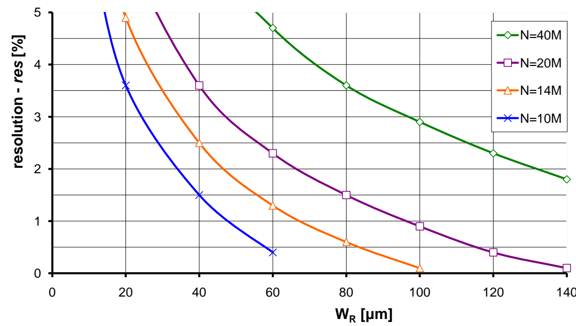

Fig. 13. Defective current resolution with respect to current mirror transistor width W_R for various circuit sizes N

The experimental results from the fabricated demonstration circuit confirmed that the proposed I_{DDQ} testing technique is capable to provide high fault coverage for the circuit under test avoiding yield loss.

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