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A current monitoring technique for I_{DDQ} testing in digital integrated circuits

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ABSTRACT

Although I_{DDQ} testing has become a widely accepted defect detection technique in CMOS ICs, its effectiveness in nanometer technologies is threatened by the increased leakage current variations. In this paper, a current monitoring technique that overcomes the current variations problem in I_{DDQ} testing is proposed. According to this, a core is partitioned into two subcircuits and the intrinsic leakage current of the one subcircuit is used to control the leakage current at the I_{DDQ} sensing node of the other and vice-versa during test application. This way process related leakage current variations are taken into account and small defective currents turn to be detectable according to the needs of modern nanometer technologies. Additionally, a Built-In Current Sensor is presented, which exploits the proposed technique and experimental results are illustrated by its application on a fabricated chip.

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1. Introduction

Quiescent current (I_{DDQ}) monitoring is a well established technique for testing integrated circuits (ICs) in CMOS technologies. I_{DDQ} testing is based on the assumption that the intrinsic, defect-free, quiescent current (here after called background current, I_B) of an IC is small compared to the quiescent current in the presence of a defect in the circuit. Consequently, setting the maximum current from the expected range of background currents in a Circuit (or Core) Under Test (CUT) as the threshold current, we can discriminate defect free from defective ICs by comparing their I_{DDQ} current with this threshold current. In case that the I_{DDQ} current is higher than the threshold value the circuit is characterized as defective. However, in nanometer technologies the effectiveness of the above I_{DDQ} testing process is threatened by the increased fluctuations in the value of the background current due to excess manufacturing process variations. Under these circumstances, the application of I_{DDQ} testing using a single threshold for discrimination between defect free and defective circuits is impractical since it will either lead to yield loss or reduced fault coverage. In addition, as technology scales down providing short channel, thin oxide, low threshold voltage (V_{th}) transistors, there is a significant increase in circuit background current [1–5] while in parallel the values of defective currents that are required to be detectable are decreased [2]. An estimation is that the transistor leakage current is increased by a factor of 7.5 in every technology generation [4]. In addition the number of transistors in a single chip is increased rapidly resulting in a further increase of the background current. There are various leakage generation mechanisms that contribute to the total transistor leakage current, like the subthreshold current, the junction leakage, the gate tunneling current, the drain induced barrier lowering (DIBL) current or the gate induced drain leakage (GIDL) current [4,5]. Moreover, there is a number of parameters that affect transistor leakage current, like the channel length (short channel effects), the threshold voltage, the gate oxide thickness, the drain and source junction depth, the doping profile, the power supply voltage and the temperature.

Several techniques have been proposed to make I_{DDQ} testing feasible in nanometer technologies. These can be classified into two main categories: those that target background current reduction during I_{DDQ} testing and those that try to increase the immunity of I_{DDQ} testing to background current fluctuations. Starting with the first category, in [3], the transistor threshold voltage is increased by applying during testing proper substrate biasing in order to reduce the background current. In [6] the use of dual threshold voltage design techniques for the transistors at the slow paths of the CUT is discussed. An alternative way to reduce the leakage current is to apply a lower supply voltage in the quiescent state [3]. In addition, since the leakage current has an

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exponential growth with the temperature while the current due to defects is decreased with it, the application of I_{DDQ} testing at lower temperatures, where the leakage current is reduced, is reported in [3]. Next in the second category, a multi-parameter I_{DDQ} testing technique is presented in [3,7] using both the I_{DDQ} current and the IC's maximum operating frequency F_{max} to discriminate fast (low V_{th} – increased background current) dies from defective dies and achieve higher yield. In [8] the current ratio of the maximum I_{DDQ} to the minimum I_{DDQ} for a test set is used as pass/fail criterion. The current ratio is determined by characterization of fault free chips. Then, during production testing, the I_{DDQ} value for the vector that provides the minimum I_{DDQ} current is measured and is exploited, using the predetermined ratio, to predict the maximum nominal I_{DDQ} current of the chip. The predicted current value is set as the threshold during the application of the test set under consideration for I_{DDQ} testing. Another method uses a set of I_{DDQ} measurements to predict the I_{DDQ} current of each test vector; the absolute value of the difference between the measured and predicted I_{DDQ} is then used for defective circuit identification [9]. Moreover, the ΔI_{DDQ} testing technique has been introduced to increase I_{DDQ} testing quality [10–12]. According to this method, differences (delta) in I_{DDQ} measurements for consecutive test vectors for a chip are obtained. In a fault free chip the mean delta is expected to be a small non-zero value but for a defective chip this value should be much higher, providing the ability to distinguish between faulty and fault free chips. Complementary ΔIDDQ (CΔIDDQ) combines a modified test pattern generation method with a simple post-processing of I_{DDQ} measurements in order to eliminate the main current variance sources [13]. The σ–I_{DDQ} test method is proposed in [14], which integrates a variation-aware leakage estimator and a clustering algorithm to classify chips without using threshold values. In addition to the previous techniques, methods based on statistical cluster analysis [15] and variance reduction of normal leakage current within smaller wafer regions [16] or wafer-level spatial analysis [17] have been proposed. Furthermore, the neighbor current ratio (NCR) method that combines wafer-level spatial correlation and current ratios has been proposed in [18,19] to sustain I_{DDQ} testing. Moreover, considering the dependence of the leakage current on the applied input vector to the CUT [20], a method to select a proper set of I_{DDQ} test vectors has been proposed so that low background current is achieved during testing [21]. A graphical I_{DDQ} current signature is proposed in [22] where the I_{DDQ} measurements are plotted as a waveform and the discrimination of defect free from defective chips is based on the noise in this waveform.

Finally, a common practice is the partitioning of the CUT into subcircuits [23] and then the use of Built-In Current Sensors (BICS) for I_{DDQ} testing in each partition. A differential BICS design for high speed I_{DDQ} testing is proposed in [24]. Current mirrors are exploited in [25] for the design of a current mode BICS. In [26] a built-in current sensing device is presented that is based on a three stage current amplifier. A BICS circuit with adjustable reference current for I_{DDQ} current comparisons is discussed in [27]. The concept of a quiescent monitor based on the current conveyor CCII+ principle is presented in [28]. Moreover, a programmable BICS is proposed in [29], where a dedicated single transistor sensor per core in a chip is exploited along with a shared two stage amplification unit. The first stage consists of two amplifiers, a common source and a source follower and the second stage is a typical differential amplifier. In [30,31] a BICS circuit for ΔI_{DDQ} testing is proposed. Its operation is based on the conversion of a voltage drop proportional to the quiescent current into a digital word. In [32] a differential built-in current monitor for analog circuits is presented.

The I_{DDQ} testing technique proposed in this paper belongs to the second category and targets to control the background current of the CUT at the I_{DDQ} sensing node during test application, taking into account current fluctuations. Thus, simple current monitoring methods can be applicable in nanometer technologies I_{DDQ} testing. A suitable I_{DDQ} testing architecture and a built-in current sensing (BICS) circuit are also presented to support the proposed technique. A preliminary study of this testing scheme has been presented in [33] while early experimental results were discussed in [34]. In the present work the trade-off among the circuit size, the BICS cost and the defective current resolution is analyzed and complete experimental results are provided. The paper is organized as follows. In Section 2 preliminaries on I_{DDQ} testing issues and problems related to its application are discussed. Next, in Section 3 the proposed I_{DDQ} testing approach is presented and analyzed. In Section 4 experimental results from a fabricated demonstration circuit are provided and discussed. Finally in Section 5 the conclusions are stated.

2. Preliminaries

The quiescent current (I_{DDQ}) of a circuit is defined as the sum of its leakage currents (background current I_B), due to the various leakage generation mechanisms, plus any defective current (I_{DEF}), due to a possible defect in it. Fig. 1 presents a common I_{DDQ} testing scheme based on the use of a Current Sensor, either embedded to the IC (Built-In Current Sensor – BICS) or external to it. The CUT is isolated from the ground supply (Gnd) by an nMOS transistor (MN_G) while the Current Sensor is connected to the virtual ground (V_Gnd) of the CUT. During the normal mode of operation the signal *T_ENB* is high, thus the transistor MN_G is in conducting state and the V_Gnd node is grounded. In the test mode of operation the signal *T_ENB* turns low and the transistor MN_G is at the non-conducting state. The Current Sensor circuit compares the I_{DDQ} current of the CUT with a reference current (I_{REF}). In case that the I_{DDQ} current is greater than the I_{REF} current, the CUT is characterized as defective. According to the above scheme, the I_{REF} current must be greater than the maximum defect free background current I_B of the CUT. Equivalently, this I_{DDQ} testing scheme can be also applied at the side of the V_{DD} power supply.

In nanometer technologies the circuit background current I_B is increased with technology evolution. Moreover, the defective current I_{DEF} that is required to be detectable is decreased [2] increasing the difficulty to discriminate defect free and defective I_{DDQ} currents. However, the main problem of I_{DDQ} testing in nanometer technologies is the large and increasing fluctuations in the value of I_B due to the increased process variations as technology scales down. In addition, the value of I_B is also influenced by temperature variations. Considering these fluctuations in the value of I_B, the application of I_{DDQ} testing using a

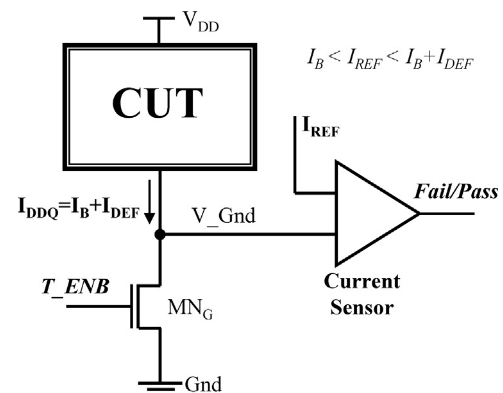

Fig. 1. A common I_{DDQ} testing scheme.

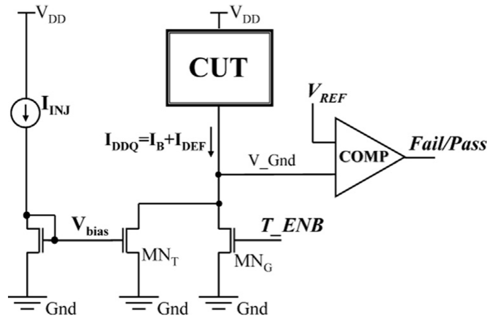

Fig. 2. The I_{DDQ} testing concept.

unique reference current I_{REF} for the discrimination between defect free and defective circuits for all chips in a production line, turns to be impractical since under these circumstances the test process will either lead to reduced fault coverage or yield loss. Consequently, I_{REF} must be adjusted for each chip in order to take into account process variations. This is a very hard task, if not infeasible.

An alternative technique to perform I_{DDQ} testing is illustrated in Fig. 2. An extra transistor MN_T is added between the virtual ground of the CUT and the ground supply (Gnd), in parallel to the MN_G transistor. This transistor is biased with a proper voltage V_{bias} so that in the defect free case the voltage V_{V_Gnd} at the virtual ground node (V_Gnd) is less than a reference voltage V_{REF}, while in the defective case this voltage will be higher than V_{REF} due to the presence of the defective current in the CUT. A voltage comparator (COMP) is used to discriminate defect free from defective cases. In this topology the CUT and the MN_T transistor act as a current to voltage converter. The bias voltage V_{bias} can be generated in a trivial way using an injection current I_{INJ} and a current mirror. As earlier, the MN_G transistor is exploited to switch between the normal and the test mode of operation under the control of the test enable signal *T_ENB*.

However, since the background current I_B of the CUT is influenced by process and temperature variations, the injection current I_{INJ} must be accordingly adjusted (as I_{REF} in Fig. 1) in order to avoid fault coverage reduction or yield loss.

3. The proposed I_{DDQ} testing technique

Considering the I_{DDQ} testing scheme in Fig. 2 and the discussion above, we need a mechanism that dynamically adjusts I_{INJ} to process and temperature variations. In this section we present a technique and a circuit to achieve this target.

3.1. Process and temperature variations immunity scheme

In order to provide the required immunity of I_{DDQ} testing against process and temperature variations we adopted the partitioning of the CUT into two subcircuits (for convenience the left subcircuit sub-CUT_L and the right subcircuit sub-CUT_R). Then the background current of the left subcircuit is used as injection current for the testing of the right subcircuit and vice-versa. Since in each case the background and the injection currents are influenced by the same process and temperature variations in the CUT, the I_{DDQ} testing process turns to be almost independent of these two factors.

In Fig. 3 the simplified block diagram of the proposed I_{DDQ} testing technique is demonstrated, where the background current of sub-CUT_L is used to generate the injection current for the I_{DDQ} testing of sub-CUT_R. A similar scheme can be also included for the I_{DDQ} testing of sub-CUT_L. For this purpose a Current Mirror Amplifier

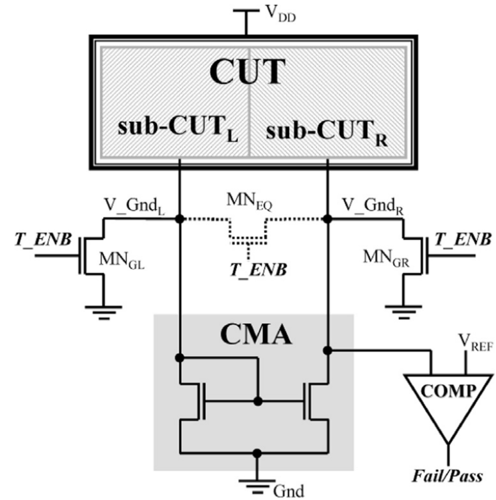

Fig. 3. The concept of the proposed I_{DDQ} testing technique.

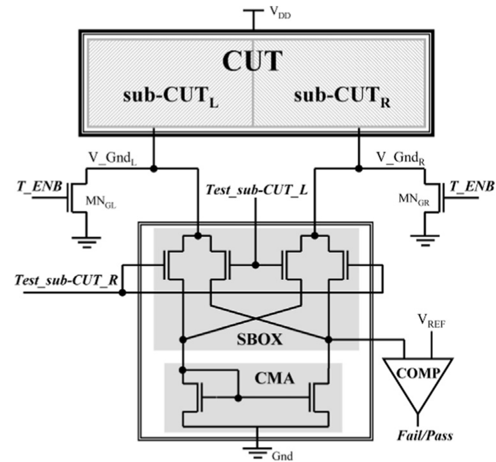

Fig. 4. The use of a single CMA for the testing of both subcircuits.

(CMA) is exploited. Each partition must have a dedicated virtual ground (V_Gnd_L and V_Gnd_R respectively). The I_{DDQ} testing circuitry (consisting of the CMA, the comparator and transistors MN_{GL} and MN_{GR}) can be either embedded in the chip along with the CUT, forming a BICS circuit, or externally of the chip as part of the Automatic Test Equipment (ATE). In the latter case, the virtual ground nodes of each partition are connected to dedicated pads that are shorted between each other during the normal mode of operation in the field. In either case, the virtual ground nodes can be also internally shorted using an equalization transistor MN_{EQ}. Note that transistors MN_{GL} and MN_{GR} can be the power gating transistors that are commonly used in modern nanometer technologies for static power reduction. Consequently, the silicon area cost of these transistors and the pertinent speed performance degradation, are exactly the same as these reported from the application of power gating techniques [35]. During I_{DDQ} testing the background current I_{BL} of sub-CUT_L is used as injection current at the CMA for the generation of the bias current $I_{BR}=\beta I_{BL}$ to test sub-CUT_R (where β is the current gain of the current mirror). As we mentioned earlier in Section 2, the sub-CUT_R and the current mirror act as a current to voltage converter. The voltage level generated at the V_Gnd_R node is compared to a reference voltage V_{REF} in order to discriminate defect free from defective circuits.

In practice, a single CMA can be used to test both subcircuits. This is achieved using a switch box (SBOX) and two control signals (*Test_sub-CUT_L* and *Test_sub-CUT_R*) as illustrated in Fig. 4. The

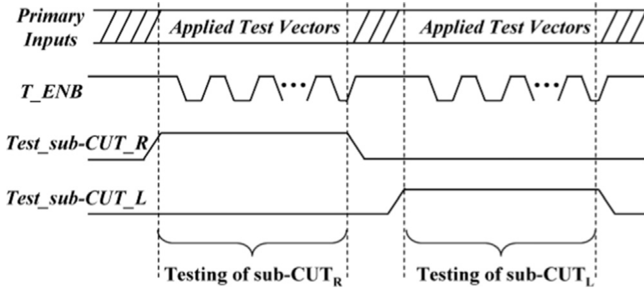

Fig. 5. I_{DDQ} testing signals' waveforms.

I_{DDQ} testing process is divided into two successive phases according to Fig. 5. The first one where sub-CUT$_L$ provides the reference current and sub-CUT$_R$ is the circuit under test using the appropriate test vectors set and the second one where sub-CUT$_R$ provides the reference current and sub-CUT$_L$ is the circuit under test using its dedicated test vectors set. A test vector, that is an input stimulus to the whole circuit, is applied by initially setting the *T_ENB* signal to high (normal mode). Then, as the circuit enters the quiescent state, the *T_ENB* signal is turned to low (testing mode) and the I_{DDQ} testing procedure is performed on the pertinent subcircuit. This operation is continued until the completion of all test vectors. During the I_{DDQ} testing of sub-CUT$_R$, the signal *Test_sub-CUT_R* is "high" while the signal *Test_sub-CUT_L* is "low". Thus, the background current I_{BL} of sub-CUT$_L$ is used as injection current for the generation of the required bias current I_{BR} for sub_CUT$_R$. The bias current for the I_{DDQ} testing of sub-CUT$_L$ is generated in the same way using the background current of sub-CUT$_R$ as injection current by turning *Test_sub-CUT_L* to "high" and *Test_sub-CUT_R* to "low". In case that a test vector is used to detect possible faults in both subcircuits, then it is applied only once to the CUT and then the signals *Test_sub-CUT_L* and *Test_sub-CUT_R* are properly treated according to the above procedure in order to test each subcircuit. Note that since in the normal mode of operation the signals *Test_sub-CUT_L* and *Test_sub-CUT_R* can take any value, a single signal and its complement can be used instead respectively. Any layout driven, I_{DDQ} oriented Automatic Test Pattern Generation (ATPG) tool can be exploited for test vector generation.

3.2. Tunable current mirror amplifier

In general the two subcircuits under consideration during I_{DDQ} testing are not identical. Consequently, their background currents I_{BL} and I_{BR} are not expected to be equal. In addition, the magnitude of each background current depends on the applied test vector. From the above it is evident that a tunable current mirror (a current mirror with tunable current gain β) is required in order to be able to generate for each test vector (j) the bias current $I_{B(L/R)j}$ from the injection current $I_{B(R/L)j}$ according to the following relation: $I_{B(L/R)j}=\beta_j I_{B(R/L)j}$. The tunability of the current mirror is not a hard constraint in the design due to the following two reasons [36]: (a) the cardinality of a test set for I_{DDQ} testing is too small and (b) there is a wide variety of alternative test vectors that can be used for the detection of each fault when I_{DDQ} testing techniques are applied. Thus, it is feasible to base the selection of the required test vectors on static (DC) power analysis [37,38] in order to reduce the background currents variations from test vector to test vector. This is not a time consuming step since it is performed only once using widely available analysis tools. Then, test vectors providing neighboring values of background current in each subcircuit are grouped together. This way the tunability requirements of the current mirror are restrained. According to this approach each group of test vectors is accompanied by the identification of the proper state (current gain) for the current mirror. Possible differences, due to process or temperature variations, between the simulated and the actual (in the field) background currents of the CUT are expected not to invalidate the method since these variations affect in the same way both background currents. Thus, the required current gain β remains almost unaltered.

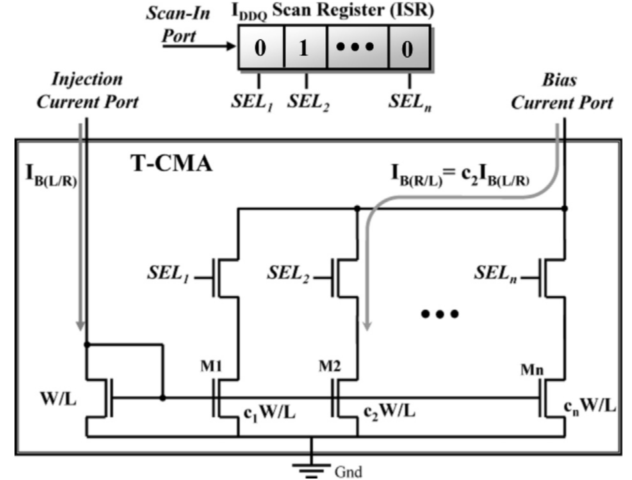

Fig. 6. A tunable current mirror amplifier (T-CMA).

A simple scheme to implement a tunable current mirror amplifier (T-CMA) is illustrated in Fig. 6. In this design multiple parallel current mirrors are used as current amplifiers in order to generate the appropriate bias current $I_{B(R/L)}$ for the I_{DDQ} testing of the corresponding sub-CUT$_{(R/L)}$. The current mirrors act as current sinks at the virtual ground of this subcircuit. The injection current is mirrored through a variety of different size sinking transistors (M_1–M_n). Each sinking transistor is characterized by its width W_i (where $i \in (1 \ldots n)$) and provides a unique amplification coefficient c_i that has an individual contribution to the bias current generation. Furthermore, a transistor in series to each sinking transistor is used as select device to activate the pertinent branch and provide the ability to synthesize the proper bias current for each test vector that is applied to the CUT.

As we mentioned earlier, a flexible technique to exploit the above I_{DDQ} testing scheme is to group together test vectors of the test set according to the required bias current. Then, a scan register (I_{DDQ} Scan Register – ISR) can be utilized with as many stages as the number (n) of the current mirror branches. The output of each stage drives a distinct select transistor. The ISR can be part of the CUT's scan chain or a user defined test register of the IEEE 1149.1 boundary scan or the IEEE 1500 embedded core testing standards [39]. To be more precise the ISR must have two more stages for the *Test_sub-CUT_L* and the *Test_sub-CUT_R* signals which determine the subcircuit under test. During I_{DDQ} testing and for each group of test vectors a dedicated pattern (activation vector) is shifted in the ISR. The activation vector determines which branches of the current mirror will be activated according to the bit positions with logic value "high". Thus the required current gain $\beta_{(L/R)}$ is provided by the sum of the amplification coefficients (c_i) of the active current mirror branches ($\beta_{(L/R)}=\Sigma c_i$). Selecting properly the size of the sink transistors, the tunable current mirror can generate the required bias currents.

3.3. Circuit partitioning

An essential requirement of the proposed I_{DDQ} testing technique (either using an embedded BICS circuit or an external to the chip circuitry) is the partitioning of the CUT into two subcircuits. According to the above discussion, each subcircuit has a power

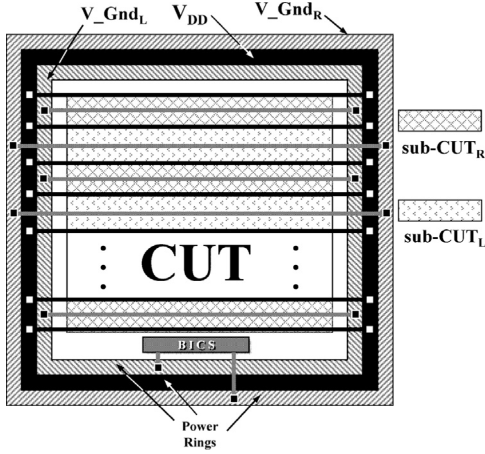

Fig. 7. The proposed power supply partition technique for a core.

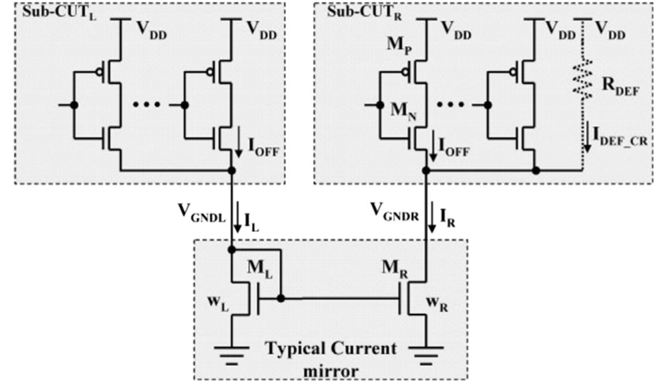

Fig. 8. The circuit model used in the study.

supply rail that is dedicated to it (in Fig. 4 this is the ground supply rail V_Gnd) while the second power supply rail (V_{DD}) is common to both subcircuits. A primary target of the partitioning scheme is to obtain in both subcircuits equivalent dependence of their background currents on process and temperature variations, in order to provide immunity of the proposed I_{DDQ} testing technique to these parameters. A possible ground supply partitioning technique is illustrated in Fig. 7. According to this scheme two independent ground rails (V_Gnd$_L$ and V_Gnd$_R$) are interdigitated inside the CUT in order to provide the ground supply to it. During the normal operation in the field the two rails are short-circuited (internal switches can be used as shown in Fig. 3). The parts of the CUT with common ground rail constitute a subcircuit (sub-CUT). This way, we expect that local process and temperature variations affect both subcircuits during I_{DDQ} testing. Note that it is not a prerequisite that the two subcircuits must present similar sizes. However, from a statistical point of view, it is not expected that the sizes of the two subcircuits will substantially vary between each other when the above partitioning scheme is followed.

3.4. Circuit partitioning and current resolution in a BICS implementation

Given that a CUT has been partitioned, an external or an embedded I_{DDQ} testing circuit according to the topology of Fig. 3 can be realized. However, especially in case of an embedded I_{DDQ} testing scheme (e.g. a BICS circuit), the tradeoff among the size of BICS circuit, the size of the CUT and the desired defective current resolution should be taken into account. The defective current resolution is defined as the minimum amount of defective current that the sensor can distinguish [30]. In this section the above tradeoff is calculated and discussed.

For simplicity, the CUT is modeled as a circuit of N inverters of the same transistor sizes, as it is shown in Fig. 8. It is partitioned into two subcircuits, sub-CUT$_L$ and sub-CUT$_R$, with N_L and N_R inverters respectively ($N=N_L+N_R$). The BICS consists of a typical current mirror. The comparator and the SBOX are not present in this figure. A defect is modeled as a resistance R_{DEF} between V_{DD} and V_{GNDR}.

We assume that the absolute values of the pMOS and nMOS threshold voltages are equal. Moreover, the nMOS transistors in each inverter have the minimum technology size ($W_N=W_{min}$), while the size of the pMOS transistors are α times greater ($W_P=\alpha W_N$) so that under the same voltage conditions both transistors present equal drain currents. Consequently, the leakage current of a pMOS transistor (in an inverter where its input is high) is equal to the leakage current of an nMOS transistor (in an inverter where its input is low). Thus, for simplicity but without loss of generality, for each inverter in the circuit the leakage current formula of the nMOS transistor can be considered to express the contribution of the gate to the circuit background current. The subthreshold leakage current (I_{OFF}) of an nMOS transistor is given by the following equation [40]:

$$I_{OFF}=\mu_n C_{OX}\frac{W}{L}V_T^{\,2}e^{1.8}e^{(V_{GS}-V_{th0}+\eta V_{DS}+\gamma V_{BS})/n\cdot V_T}\left(1-e^{-(V_{DS})/V_T}\right) \quad (1)$$

where V_{GS}, V_{DS} and V_{BS} denote the gate, drain and bulk to source voltage respectively, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the effective transistor width and length respectively, V_{th0} is the zero bias threshold voltage, V_T is the thermal voltage, n is the subthreshold swing coefficient, η is the DIBL coefficient and γ is the linearized body effect coefficient.

Now, considering an nMOS transistor like M_N in an inverter of Fig. 8 and the assumption that its gate is driven to low by another inverter, the following equations hold for the transistor's voltages: (a) $V_{GS}=0$ (since a low input signal refers to a voltage equal to V_{GNDR}), (b) $V_{DS}=V_{DD}-V_{GNDR}$ and (c) $V_{BS}=0-V_{GNDR}=-V_{GNDR}$ (considering that the bulk is grounded, else $V_{BS}=0$ when the bulk is connected to V_{GNDR}). Thus, according to Eq. (1) the leakage current of this transistor is expressed as follows:

$$I_{OFF}=\mu_n C_{OX}\frac{W}{L}V_T^{\,2}e^{1.8}e^{(-V_{th0}+\eta(V_{DD}-V_{GNDR})-\gamma V_{GNDR})/(n\cdot V_T)}\left(1-e^{-(V_{DD}-V_{GNDR})/V_T}\right) \quad (2)$$

Next, given that the transistor M_R of the current mirror operates in the saturation region, its drain current is expressed by the equation that follows:

$$I_{DR}=\frac{\mu_n C_{OX}}{2}\frac{W_R}{L}(V_{GSR}-V_{th})^2(1+\lambda V_{DSR}) \quad (3)$$

where W_R and L are the transistor's width and length, V_{GSR}, V_{DSR} are the gate and drain to source voltage respectively, V_{th} is the threshold voltage and λ is the channel-length modulation parameter. It stands that

$$V_{th}=V_{th0}+\gamma'\left(\sqrt{|-2\Phi+V_{SB}|}-\sqrt{|2\Phi|}\right) \quad (4)$$

where γ' is the body effect coefficient and Φ is the Fermi potential.

For transistors M_L and M_R in the current mirror of Fig. 8 it stands that $V_{GSR}=V_{GSL}\equiv V_{GNDL}$. Moreover, $V_{DSR}\equiv V_{GNDR}$. Consequently, Eq. (3) can be rewritten as follows:

$$I_{DR}\equiv I_R=\frac{\mu_n C_{OX}}{2}\frac{W_R}{L}(V_{GNDL}-V_{th})^2(1+\lambda V_{GNDR}) \quad (5)$$

In the equilibrium we can write

$$I_{DR} = I_R = N_R I_{OFF} \tag{6}$$

Substituting Eqs. (2) and (5) in (6) we get:

$$\frac{W_R}{2}(V_{GNDL} - V_{th})^2(1+\lambda V_{GNDR}) = N_R W V_T{}^2 e^{1.8} e^{(-V_{th0} + \eta(V_{DD} - V_{GNDR}) - \gamma V_{GNDR})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{GNDR})/V_T}\right) \tag{7}$$

In general $N_L = s.N_R$ (with s any real number), however without loss of generality let us consider that $N_L = N_R = N/2$. Then, setting $W_L = W_R$, it results that I_L will be equal to I_R ($I_L = I_R = NI_{OFF}/2$) and $V_{GNDR} = V_{GNDL}$. Thus, Eq. (7) is rewritten as follows:

$$W_R(V_{GNDR} - V_{th})^2(1+\lambda V_{GNDR}) = NWV_T{}^2 e^{1.8} e^{(-V_{th0} + \eta(V_{DD} - V_{GNDR}) - \gamma V_{GNDR})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{GNDR})/V_T}\right) \tag{8}$$

According to the I_{DDQ} testing scheme in Fig. 3 a comparator is used to discriminate defect free from defective circuits. In case that the voltage V_{GNDR} is less than a reference voltage V_{REF} then the right subcircuit is characterized as defect free else it is defective. Consequently, for a given reference voltage V_{REF} and setting $V_{GNDR} = V_{REF}$ in Eq. (8) we can determine the transistor width W_R in the current mirror that should be used for a given circuit size N or we can estimate the size N of the CUT that a current mirror is capable to support for a given transistor width W_R, as follows:

$$\frac{W_R}{N} = \frac{WV_T{}^2 e^{1.8} e^{(-V_{th0} + \eta(V_{DD} - V_{REF}) - \gamma V_{REF})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{REF})/V_T}\right)}{(V_{REF} - V_{th})^2(1+\lambda V_{REF})} \tag{9}$$

In what follows we will examine how process variations affect the above calculations. Note that along with the CUT, also the current mirror is exposed to these variations. As it is proved from Eq. (8), assigning to the pertinent parameters the values of a high leakage process corner of a technology (usually referred as fast process corner) V_{GNDR} is increased, while assigning the parameters of a low leakage process corner (slow process corner) V_{GNDR} is decreased. Next, suppose that we use Eq. (9) to determine W_R for a given N in the typical process condition. Then, in the fault free case and considering the two edge corners, fast and slow, we observe that (a) for a CUT in the fast corner the voltage V_{GNDR} will be higher than V_{REF} leading to yield loss (since the circuit is identified as defective) and (b) for a CUT in the slow corner the voltage V_{GNDR} will be lower than V_{REF} leading to a lower defect coverage. The latter stems from the fact that a lower defect resistance (a hard defect) is required to raise the voltage in V_{GNDR} higher than V_{REF} in order this defect to be detectable (which means that light defects turn to be undetectable). Thus, the width W_R for a given CUT size N, a given reference voltage V_{REF} and a given defective current resolution must be determined taking into account process variations.

Eq. (10) expresses the relative defective current resolution:

$$res = \frac{I_{DEF}}{I_B} \times 100\% \tag{10}$$

where I_{DEF} is the defective current due to the maximum detectable defective resistance R_{DEF} (thus this is the minimum detectable defective current) and I_B is the corresponding fault free background current of the circuit. In I_{DDQ} testing we want the resolution to be as small as possible so that small defective currents, or in other words high defective resistances (lighter defects), are detectable. Obviously, for a given CUT and BICS the worst resolution appears in the slow process corner where I_B takes the smallest value according to Eq. (1).

Initially, in order to avoid yield loss during the application of the I_{DDQ} testing procedure on a CUT with size N, we define W_R from Eq. (9) so that the voltage V_{GNDR} in the fast process corner is equal to V_{REF} ($V_{GNDR_FA} = V_{REF}$). Consequently, in Eq. (9) the technology parameters of the fast process corner are used to define W_R.

$$W_R = \frac{NWV_T{}^2 e^{1.8} e^{(-V_{th0_FA} + \eta(V_{DD} - V_{REF}) - \gamma_{FS} V_{REF})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{REF})/V_T}\right)}{(V_{REF} - V_{th_FA})^2(1+\lambda V_{REF})} \tag{11}$$

Next, for the above transistor width we will determine the achieved relative resolution. However, first we have to calculate V_{GNDR} for the slow process corner (V_{GNDR_SL}). Again, it stands that $V_{GNDL_SL} = V_{GNDR_SL}$. Towards this direction, we exploit Eq. (8) using the above defined W_R and the technology parameters of the slow corner as follows:

$$W_R(V_{GNDR_SL} - V_{th_SL})^2(1+\lambda V_{GNDR_SL}) = NWV_T{}^2 e^{1.8} e^{(-V_{th0_SL} + \eta(V_{DD} - V_{GNDR_SL}) - \gamma_{SL} \cdot V_{GNDR_SL})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{GNDR_SL})/V_T}\right) \tag{12}$$

From Eq. (12) it is difficult to find an analytical expression for V_{GNDR_SL}. However, it is feasible to solve this equation for V_{GNDR_SL} using arithmetic methods provided by various tools like Maple [41].

According to (10), for the calculation of the achieved relative resolution we have to define initially the worst case (minimum) detectable defective current I_{DEF} in the normal mode of the CUT operation, which is the defective current without the presence of the current mirror. This corresponds to the maximum detectable defective resistance R_{DEF} (see Fig. 8) and $I_{DEF} = V_{DD}/R_{DEF}$. However, note that in the presence of the current mirror a defective current I_{DEF_CM} flows through R_{DEF} instead of I_{DEF}. In order this defective resistance to be detectable in all process corner conditions, we have just to ensure that it is detectable in the slow process corner. The latter stems from the fact that in this corner the virtual ground of the right subcircuit has the minimum voltage V_{GNDR_SL}. In that case, the presence of R_{DEF} must be capable to raise the virtual ground of the right subcircuit from V_{GNDR_SL} to just above (at the limit up to) V_{REF} in order to detect the corresponding defect. In the equilibrium where $V_{GNDR} = V_{REF}$ it stands

$$I_{DEF_CM} = I_{DR_SL_DEF} - \frac{N}{2} I_{OFF_SL_DEF} \tag{13}$$

where $I_{DR_SL_DEF}$ is the drain current of transistor M_R in the presence of the fault and is calculated using Eq. (5) for the slow corner, setting $V_{GS} = V_{GNDL_SL}$ and $V_{DS} = V_{REF}$:

$$I_{DR_SL_DEF} = \frac{\mu_{n_SL} C_{OX_SL}}{2} \frac{W_R}{L} (V_{GNDL_SL} - V_{th_SL})^2 (1+\lambda V_{REF}) \tag{14}$$

while $I_{OFF_SL_DEF}$ is the transistor leakage current in the faulty case, which is calculated using Eq. (2) for the slow corner by setting $V_{GNDR} = V_{REF}$:

$$I_{OFF_SL_DEF} = \mu_{n_SL} C_{OX_SL} \frac{W}{L} V_T{}^2 e^{1.8} e^{(-V_{th0_SL} + \eta(V_{DD} - V_{REF}) - \gamma_{SL} \cdot V_{REF})/(n \cdot V_T)} \left(1 - e^{-(V_{DD} - V_{REF})/V_T}\right) \tag{15}$$

Thus the maximum detectable defective resistance R_{DEF} in all process corners is determined as follows:

$$R_{DEF} = \frac{V_{DD} - V_{REF}}{I_{DEF_CM}} \tag{16}$$

Now we can calculate the minimum detectable defective current I_{DEF} in the normal mode, that is

$$I_{DEF} = \frac{V_{DD}}{I_{DEF}} = \frac{V_{DD}}{V_{DD} - V_{REF}} I_{DEF_CM} \tag{17}$$

Next, the corresponding background current I_B of the CUT can be calculated using Eq. (1) for the transistor leakage current in the

slow corner setting $V_{GS}=V_{BS}=0$, $V_{DS}=V_{DD}$, $I_B=NI_{OFF}$:

$$I_B = N\mu_{n_SL}C_{OX_SL}\frac{W}{L}{V_T}^2 e^{1.8} e^{(-V_{th0_SL}+\eta V_{DD})/(n\cdot V_T)}\left(1-e^{-V_{DD}/V_T}\right) \quad (18)$$

Finally, substituting I_{DEF} from Eq. (17) and I_B from Eq. (18) in Eq. (10) we can estimate the BICS relative defective current resolution *res* for the given CUT of size *N*, the selected reference voltage V_{REF} and the calculated current mirror transistor width W_R.

The above calculations provide an estimation of the worst case relative defective current resolution expected that is the resolution of a fabricated circuit at the slow corner. However, this estimation is very pessimistic since any circuit at a different process condition will present a better resolution, with the best at the fast corner. Since we select V_{REF} to be equal to the V_{GNDR} voltage in the fast corner ($V_{REF}=V_{GNDR_FA}$), it is implied from the previous discussion that the worst case relative resolution is improved (minimized) as the difference of the V_{GNDR} voltage in the slow corner from the reference voltage V_{REF} is reduced ($V_{REF}-V_{GNDR_SL}\rightarrow 0$). As this deference decreases, a smaller defective current I_{DEF_CM} is required to raise V_{GNDR} from V_{GNDR_SL} to V_{REF} and consequently according to (17) a smaller defective current I_{DEF} in the normal mode of operation is detectable.

From Eq. (8) we can prove that the difference $V_{GNDR_FA}-V_{GNDR_SL}$ decreases as the size *N* of the CUT is decreased or as the current mirror width W_R is increased. However, since *N* is a constant for a given CUT, it is feasible to decrease this difference by increasing the number of partitions in the CUT. Thus, in order to achieve a predetermined defective current resolution there is a tradeoff between the number of CUT partitions and the silicon area cost (expressed by W_R) of the BICS.

Next we apply the previous analysis using the parameters of an industrial 180 nm CMOS technology in order to have a quantitative estimation of the trade-off between *N* and W_R variables. The nominal technology parameters are shown in Table 1. The voltage supply V_{DD} is 1.8 V and the reference voltage under consideration is $V_{REF}=0.9$ V. In Fig. 9a the relative defective current resolution *res* with respect to the circuit size *N* for various current mirror transistor widths W_R is presented. It is obvious that as the circuit size is increased, a desired relative defective current resolution can be achieved by increasing the current mirror transistor widths. Equivalently, in Fig. 9b the relative defective current resolution as a function of the transistor widths in the current mirrors is presented for various circuit sizes. In addition, in Fig. 10 the required current mirror transistor widths with respect to the circuit size *N* (or equivalently the expected background current I_B) for various defective current values I_{DEF} that must be detectable (absolute defective current resolution) is presented.

4. Experimental results

4.1. Large core design and simulation results

In order to validate the proposed I_{DDQ} testing technique a demonstration circuit has been designed in a standard 180 nm CMOS technology ($V_{DD}=1.8$ V). The circuit consists of a digital core that is the circuit under test and the BICS circuit consisting of a tunable current mirror and a voltage comparator. The Virtuoso design environment of CADENCE was used.

4.1.1. The digital core

The digital core is constructed of 8×10^6 two input NAND and 8×10^6 two input NOR gates, with a total of 64×10^6 transistors which correspond to 157×10^6 unit size (minimum size) transistors ($W=0.28$ μm and $L=0.18$ μm) in the technology under consideration. The core is partitioned into two subcircuits following the ground supply partitioning technique shown in Fig. 7. Each subcircuit contains half of the total core gates of each type. Moreover, in order to achieve realistic operating conditions, each subcircuit is composed of four blocks and each block contains 1×10^6 NOR gates and 1×10^6 NAND gates so that (i) the gates of the first block have proper stable inputs to provide the maximum leakage current, (ii) the gates of the second block have proper stable inputs to provide the minimum leakage current, (iii) the gates of the third block have proper stable inputs to provide a medium leakage current and (iv) in the fourth block all the NOR gates are driven by a dedicated pair of signals and the same stands for all the NAND gates. These pairs of signals (a total of eight signals for both subcircuits) are independent to each other and externally controlled, providing 256 input combinations. In practice,

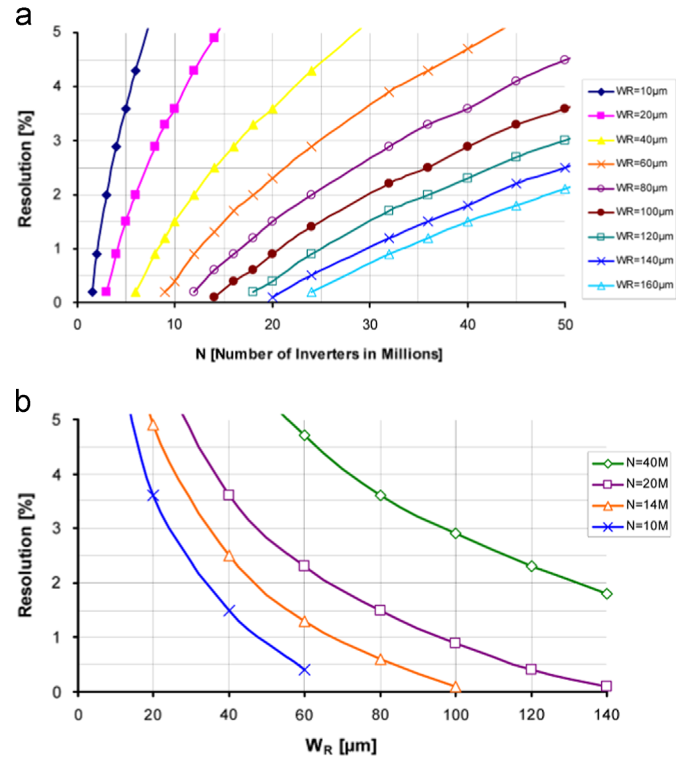

Fig. 9. (a) Defective current resolution with respect to circuit size *N* for various current mirror transistor widths W_R. (b) Defective current resolution with respect to current mirror transistor width W_R for various circuit sizes *N*.

Table 1
Technology parameters.

	Threshold voltage nMOS	Subthreshold swing coefficient	DIBL coefficient	$\mu_n C_{OX}$ product	Linearized body effect coefficient	Channel-length modulation parameter
Symbol	(V_{th})	(n)	(η)	($\mu_n C_{OX}=k'$)	(γ)	(λ)
Unit	V	–	–	A/V^2	–	V^{-1}
Value	0.37	1.43	$6.918\cdot10^{-4}$	$1.363\cdot10^{-4}$	0.04	0.224

there is not any specific functionality for the digital core since the functionality of the CUT is not important for the demonstration. In contrary, we are aiming to gain a wide controllability on the leakage current of each subcircuit by setting the gates of the fourth block to any desired state. As it is known, the leakage current of a CMOS gate depends on the state of its inputs [1,20].

Although, both subcircuits are identical this does not alter the validation procedure since great current imbalance, up to 13.5 times, can be achieved between the two subcircuits of our design by properly selecting the input vectors of each subcircuit.

4.1.2. The tunable current mirror

The heart of the BICS circuit is the tunable current mirror/amplifier (T-CMA) that is illustrated in Fig. 11. It is based on the Wilson current mirror topology which has been selected for its high output resistance [42]. The T-CMA consists of 16 branches, six branches at the side of the injection current port (ICP), that is $n=6$, and 10 at the side of the bias current port (BCP), that is $m=10$. Sixteen select signals (SEL_1–SEL_{16}), one for each branch, are exploited to provide the tunability of the current mirror. These signals drive the select transistors MS_1–MS_{16} and the corresponding CMOS switches in each branch. The widths of the current mirror's transistors M_{11}–M_{162} have been properly selected, after electrical simulations for every input combination at the inputs of the core and for every process corner of the used technology, in order to generate the desired bias currents. The transistor widths (W) are shown in Table 2, while the length (L) of all transistors is equal to 1 μm in order to reduce the impact of process variations. The width of the select transistors is equal to 30 μm while in the CMOS switch the width of the pMOS transistor is equal to 2 μm and this of the nMOS transistor is equal to 1 μm.

Note that due to possible inaccuracies in the current mirrors, which are related to transistors mismatches, various layout design techniques, like these presented in [43], have been followed here in order to cope with local process gradients, channel length modulation and devices mismatching.

4.1.3. The voltage comparator

The voltage comparator is based on a simple differential amplifier. It has been selected for its very high input resistance in order to avoid any disturbance in the generated bias current of the T-CMA by sinking current from the sensing node. Obviously, any embedded or external voltage comparator can be used. One

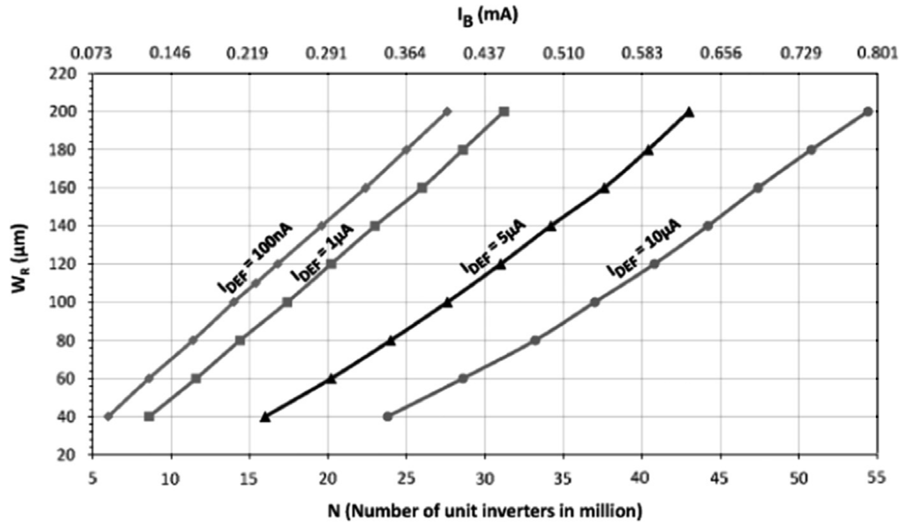

Fig. 10. Current mirror transistor widths W_R with respect to circuit size N (background current I_B) for various detectable defective current values (absolute defective current resolution).

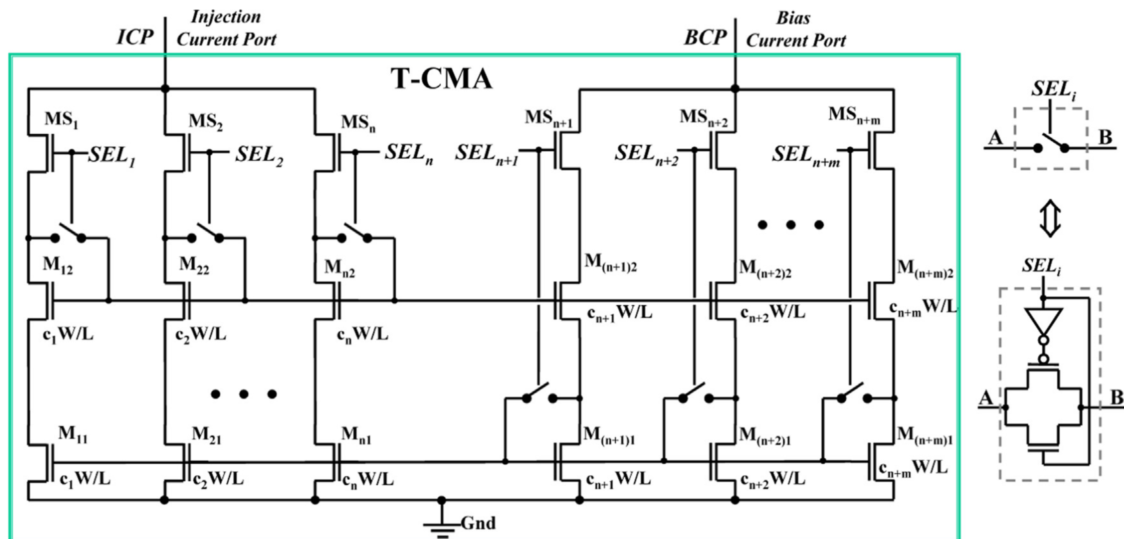

Fig. 11. The proposed T-CMA circuit and the CMOS switch.

Table 2
T-CMA transistor widths.

Transistors	LEFT branch transistor size (μm)	Transistors	Right branch transistor size (μm)
M_{11}, M_{12}	200	M_{71}, M_{72}	200
M_{21}, M_{22}	100	M_{81}, M_{82}	100
M_{31}, M_{32}	50	M_{91}, M_{92}	50
M_{41}, M_{42}	20	M_{101}, M_{102}	20
M_{51}, M_{52}	20	M_{111}, M_{112}	20
M_{61}, M_{62}	10	M_{121}, M_{122}	10
		M_{131}, M_{132}	5
		M_{141}, M_{142}	2
		M_{151}, M_{152}	2
		M_{161}, M_{162}	1

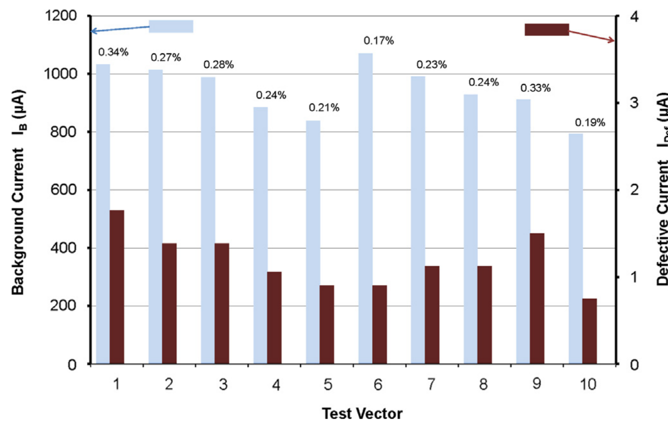

Fig. 12. Background currents, detected defective currents and defective current resolutions for 10 test vectors.

of the comparator's inputs is connected to the *BCP* port of the T-CMA and the other to a reference voltage V_{REF}. During I_{DDQ} testing, the comparator provides at its digital (fault indication) output *Fail/Pass* a "high" response in case that a fault is present (the voltage at the sensing node is higher than V_{REF}) and a "low" response in the fault free case (the voltage at the sensing node is lower than V_{REF}).

The required silicon area for the T-CMA circuit and the voltage comparator is less than 1% of the area of the core under test. However, as we mentioned earlier, it is not necessary for the proposed technique any of these two circuits to be embedded in the chip along with the CUT. This alternative may provide a higher flexibility in the design of the test circuitry. The only requirement is the proper partitioning of the CUT.

4.1.4. Simulation results

In the simulations the SPECTRE environment was used. The maximum background current of the core is 1.07 mA. Current imbalances between the two sub-circuits up to 13.5 times were considered in the simulations by exploiting the 256 input combinations of the digital circuit. The worst relative defective current resolution is 0.34% which corresponds to a defective resistance of 1 MΩ or a defective current of 1.765 μA. In Fig. 12 the background currents and the detectable defective currents for 10 test vectors with the worst relative defective current resolution are presented. The relative defective current resolution is quoted at the top of the bars. The defective resistances range between 1 MΩ and 2.4 MΩ.

Aiming to evaluate the impact of local process variations on the efficiency of the proposed BICS circuit, Monte-Carlo analysis was performed (1000 runs), exploiting the statistical models of the used technology and considering both process variations and device mismatches. According the results, where the above reported worst relative defective current resolution is maintained, the test escapes were at the range of 1‰ while the yield loss was zero.

BICS circuits presented in the literature [24–29] do not incorporate mechanisms to face background current fluctuations due to process variations or the applied test vector. In [30,31], inter-die background current variations are considered but not the dependence of the background current on intra-die (local) process variations and the applied test vector. The circuit partitioning technique and the tunable current mirror proposed in the present work provide a BICS circuit that takes into account these background current variations in order to achieve the desirable relative and absolute defective current resolutions.

4.2. I_{DDQ} test chip: design and experimental results

Aiming to further validate the proposed technique, a demonstration chip was fabricated that was a smaller version of the above circuit due to limitations in the available silicon area (1 mm^2).

4.2.1. Chip design and simulations

The core consists of 10,800 two input NAND and 10,800 two input NOR gates, that is a total of 86,400 transistors which correspond to 199,028 unit size transistors. The core is partitioned into two subciruits. As earlier eight external signals are used to control the state of the core, thus, 256 input combinations are available. The difference is that in the current version these signals feed all the NOR and all the NAND gates in each subciruit.

The T-CMA consists of six branches, three at the side of the injection current port (ICP) and three at the side of the bias current port (BCP). The widths of the current mirror's transistors is a subset of the widths in Table 2 and more precisely 20 μm, 30 μm and 100 μm for the transistors of the three left branches respectively and 50 μm, 100 μm and 200 μm for the transistors of the three right branches respectively. Exploiting the above topology it is possible to set the T-CMA into 49 different states, which means that the T-CMA is capable to provide a total of 49 different bias currents for every injection current at its ICP port.

The voltage comparator is the same as earlier. The silicon area of the T-CMA and the voltage comparator circuitry is 2.42% of the core area.

According to the DC analysis, only 10 T-CMA states are sufficient for the I_{DDQ} testing procedure, when we consider all input combinations as test vectors. The maximum expected background current I_B of the chip for all transistors' corners and for any input combination is 10 μA. The achieved relative defective current resolution in the typical process conditions is 1.24% (which corresponds to a defective resistance of 100 MΩ or a defective current of 18 nA with the background current equal to 2.9 μA) and the test application time is 300 μs, when a reference voltage of 900 mV is used. In the worst case corner the relative defective current resolution is 2.40% (which corresponds to a defective resistance of 135 MΩ or a defective current of 13 nA with the background current equal to 1.03 μA) for the same reference voltage. These are the worst case resolutions among all input combinations. Although better defective current resolutions can be achieved with slight modifications in the T-CMA circuit, the provided absolute defective current resolutions, which are in the order of few nano-amperes, is more than adequate.

Table 3
Test vector distribution per activation vector.

Activation vector $\langle SEL_1 - SEL_6 \rangle$	T-CMA amplification factor ($\beta = \Sigma c_i$)	Number of test vectors
⟨100–110⟩	300/20	2
⟨010–100⟩	100/30	10
⟨010–010⟩	200/30	32
⟨001–001⟩	50/100	24
⟨001–100⟩	100/100	129
⟨001–101⟩	150/100	1
⟨001–010⟩	200/100	32
⟨001–110⟩	300/100	4
Total test vectors		234

When the above simulations are repeated using the standard I_{DDQ} testing scheme in Fig. 2, with a proper (but fixed for all process corners) injection current per test vector and a reference voltage of 900 mV, the worst corner relative defective current resolution turns to be unacceptable, rising above 100%, due to the inability of this topology to take into account the process variations.

In addition, a second version of the chip has been considered, where ground pads have been attached to the virtual grounds (V_Gnd$_{L/R}$). The T-CMA and the voltage comparator are the same as above. This design approach is highly desirable since it will alleviate the need for large size ground isolation transistors ($MN_{GL/R}$ in Fig. 4), improving this way the core's speed performance and reducing the noise at the ground supply during the normal mode of operation. However, in that case the reference voltage is limited by the cut-off voltage of the ESD protection diodes that are used in the ground pads.

According to the new simulations, a proper set of activation vectors is presented in Table 3 along with the achieved amplification factors (β) in the T-CMA and the number of the corresponding test vectors they serve. From the total 256 input combinations the 234 combinations can be used as test vectors. The rest 22 combinations set the sensing node (V_{GNDR}) above the used reference voltage of 470 mV in the fault free case and they are discarded since they result in yield loss. The achieved relative defective current resolution in the typical process conditions is 1.90% which corresponds to a defective resistance of 42 MΩ or a defective current of 42.8 nA with the background current equal to 2.9 μA. In the worst case corner the relative defective current resolution is 5.68% (which corresponds to a defective resistance of 4 MΩ or a defective current of 450 nA with the background current equal to 10.93 μA).

4.2.2. Measurements

The second version of the chip, which includes the pads at the virtual grounds, has been fabricated in a multi-partner run. From a total of 25 chips, three were delivered to us and measured. The microphotograph of the demonstrator is shown in Fig. 13. The chip characteristics are provided in Table 4.

For the evaluation of the proposed I_{DDQ} testing technique the subset of activation vectors in Table 3 is used. A certain activation vector is applied for each group of test vectors, as it has been determined by the simulations above and it is indicated in this table (the total number of the used test vectors is equal to 234). Faulty cases are emulated by placing external resistors between the power supply pad V_{DD} and the virtual ground pads. The evaluation procedure, which has been followed for every test vector and a variety of bridging fault resistance values, is separated into two subsequent phases as follows:

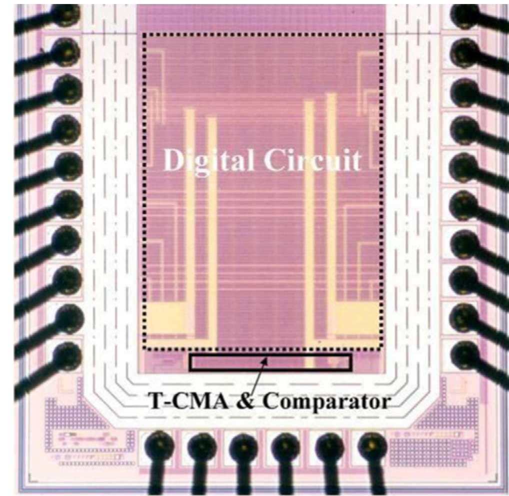

Fig. 13. I_{DDQ} test chip microphotograph.

Table 4
Chip characteristics.

Technology	CMOS 180 nm
V_{DD}	1.8 V
Chip area with pads	1 mm^2
Core area	0.48 mm^2
BICS area	0.0116 mm^2
Maximum background current I_{Bmax}	3.4 μA
Absolute defective current resolution	75 nA
Relative defective current resolution	3%

Phase 1. Fault free case – T-CMA active.
1.a. Initially, for each test vector the *T_ENB* is set to “high” and the corresponding activation vector is applied.
1.b. After the application of a test vector, the *T_ENB* is turned to “low” and the *Fail/Pass* signal is observed.

The first phase checks if the test result is always a correct fault free indication in the fault free case, when a single reference voltage is used and the proposed I_{DDQ} testing technique is applied. The experimental results confirmed that this is true for every one of the 234 test vectors used. Consequently, the proposed I_{DDQ} testing technique avoids any yield loss.

Phase 2: Faulty case – T-CMA active.
2.a. Next, for each test vector the *T_ENB* is turned back to “high”, the corresponding activation vector remains active and a bridging fault resistance is inserted.
2.b. Then, the *T_ENB* is set to “low” and the *Fail/Pass* signal is observed.

The second phase checks the existence of at least one test vector, which provides a fault detection indication in the faulty case, when a single reference voltage is used and the proposed I_{DDQ} testing technique is applied. The experimental results confirmed the existence of such test vectors for resistance values at least up to 24 MΩ for all fabricated test chips (which corresponds to a relative defective current resolution of 3% and an absolute defective current resolution of 75 nA). The above two phases indicate that the proposed I_{DDQ} testing technique is capable to provide high fault coverage for the circuit under test, avoiding yield loss. In the logic analyzer view of Fig. 14 the two subsequent phases for a test vector that is applied to the CUT are illustrated.

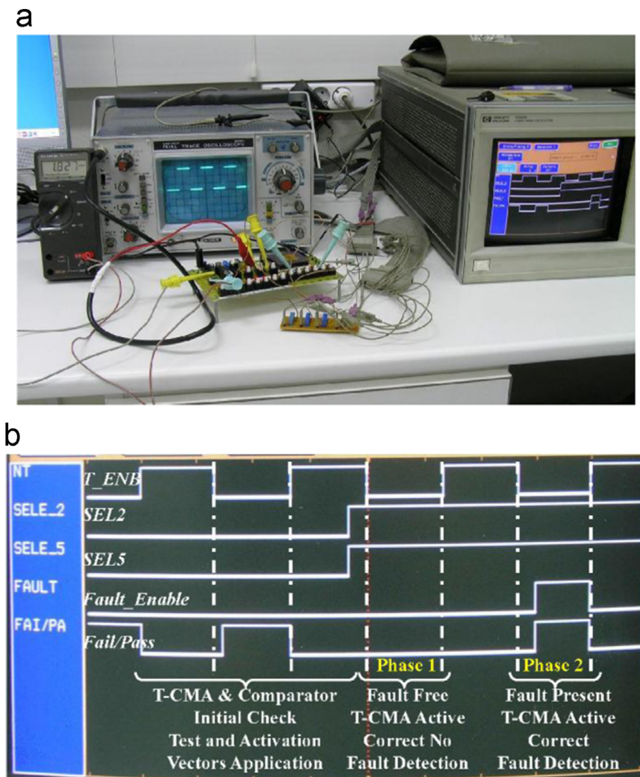

Fig. 14. (a) Test set-up and (b) logic analyzer view: evaluation procedure for a test vector that is applied to a fabricated chip.

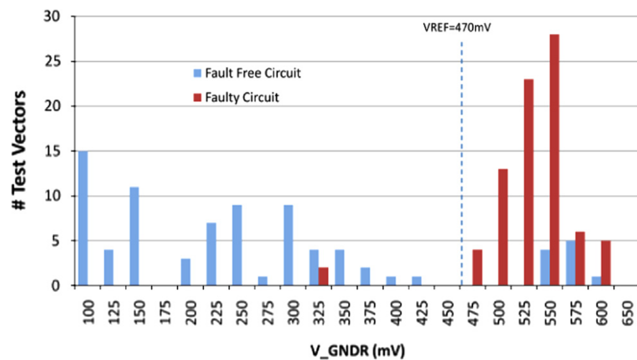

Fig. 15. Input vectors distribution with respect to the voltage level that they induce at the sensing node.

The test result was a correct “no fault detection” in the fault free case (Phase 1) and a correct fault detection in the faulty case (Phase 2).

In Fig. 15 the distribution of the input vectors with respect to the voltage level that they induce at the sensing node (V_{GNDR}) in the fault free and the faulty case is presented. A defective resistance of 10 MΩ is used. All input vectors except two are capable to detect this fault. In this figure the discarded input vectors, which raise the sensing node above the reference voltage in the fault free case, are also presented.

4.2.3. Comparisons

An efficient I_{DDQ} testing technique in the literature has been proposed in [30,31]. In this work results are also presented on an 180 nm technology for a CUT with a max background current equal to 3 μA (like in our demonstration chip). The reported relative defective current resolution is constant to 1% for background currents > 100 μA. For background currents < 100 μA the absolute defective current resolution is 1 μA (that is > 1% and increases (getting worse) rapidly as the background current is decreased – for I_B=3 μA the relative defective current resolution is 30%). Our technique presents 3% relative defective current resolution for a background current of 3 μA (in the measured chips) and 0.34% relative defective current resolution for a background current of ~1 mA (in the simulations for the large design at the worst process corner where the BICS is trimmed). Thus, we expect that the resolution is improved as the background current (circuit size) increases. Consequently, the proposed I_{DDQ} testing technique outperforms over the above solution with respect to this characteristic. Furthermore, both techniques require less than 1% additional silicon area for large functional circuits. In addition, in [30,31] the best test time equal to 400 ns/vector, for a background current of 1 mA, is reported. In our technique a typical test time is equal to 100 μs/vector, for a 3 μA background current. Although these test time results are not comparable it is expected that the speed performance of the two techniques will be the same since in both cases the test time depends on the time interval to charge/discharge the virtual ground node to a certain voltage level. Finally, the effect of the BICS on the speed performance of the CUT is expected to be the same in both techniques since this influence is exclusively related to the power switches that they use to activate the test operation.

4.2.4. Validation and limitations of the proposed approach

The measurements in Section 4.2.2 should be compared with the simulation results in the last paragraph of the Section 4.2.1, since in both cases the ground pads are attached at the virtual grounds. In the simulations as well as the measurements on the fabricated chips, we used exactly the same 234 test vectors with exactly the same activation vector per test vector according to Table 3.

Considering the simulations, in the typical process conditions the relative defective current resolution in the typical process conditions is 1.90% (which corresponds to a defective resistance of 42 MΩ or a defective current of 42.8 nA), while in the worst case process corner the relative defective current resolution is 5.68% (which corresponds to a defective resistance of 4 MΩ or a defective current of 450 nA). The BICS related circuitry of the fabricated design has been trimmed to properly operate in the worst case process corner.

In accordance to the simulations, no yield loss is reported by the measurement results while the relative defective current resolution is 3.0% (which corresponds to a defective resistance of 24 MΩ or a defective current of 75 nA). The experimental results are in compliance with the simulations. As it is stated in Section 3.4, the actual relative defective current resolution (3.0%) is definitely better than the simulated one at the worst process corner (~5.7%).

Considering the limitations of the proposed I_{DDQ} testing approach, two are the main issues. The first one is related to the increased effort required to select an appropriate set of I_{DDQ} test vectors, which will present reduced background current variations between them, in the case of an embedded implementation. Although the power supply partition technique in Fig. 7 can be exploited to reduce the effect of local process variations, these may still affect the inter-vector current variations. The second one stems from the requirement of two distinct virtual grounds instead of one as it is the case in other I_{DDQ} testing techniques. However, in modern designs the use of multiple circuit partitions

in BICS based I_{DDQ} testing seems to be imperative [23]. Along with the two virtual grounds, two activation transistors are required (transistors MN_{GL} and MN_{GR} in Fig. 4). However, these transistors can be the existing power gating transistors that are used for low static power. Independently of the transistor number, the silicon area cost is exactly the same in both cases (power transistors are distributed on the power rail).

Among the control signals that are used in the proposed technique, only the test enable signal (*T_ENB* in Fig. 4) requires a dedicated pad. However, this is the case in every BICS design, while this may be a preexisting signal in case that power gating transistors are exploited. The rest of the signals can be treated with the use of existing scan facilities. Finally, note that for the analog blocks (T-CMA, comparator) custom design techniques must be applied.

5. Conclusions

I_{DDQ} testing is a valuable manufacturing tool to achieve high defect detection levels and improve quality and reliability of CMOS ICs. However, in deep submicron technologies, the discrimination between defective and non-defective I_{DDQ} currents is hard. Thus, in order to be able to exploit I_{DDQ} benefits in circuit testing it is urgent to provide new solutions. Towards this direction, a suitable I_{DDQ} testing technique and a corresponding embedded circuit to support it are presented in this work. According to the proposed approach, during the I_{DDQ} testing application, the background current at the sensing node is properly controlled taking into account possible manufacturing process and temperature variations as well as the dependence of the background current on the applied test vector. The adoption of this method is a promising way to extend the viability of I_{DDQ} testing in future nanometer technologies.

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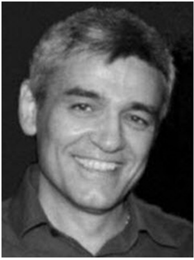

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