A Current Mode, Parallel, Two-Rail Code Checker

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Abstract—A current mode periodic output parallel two-rail code (TRC) checker, suitable for the implementation of high fan-in embedded checkers, is presented. The new checker is characterized by high testability, high-speed operation, and low silicon area requirements. The circuit has been designed, for various fan-in values, in a 0.18μm technology, and electrical simulations have been carried out to validate its operation, considering process, power supply, and temperature variations as well as variations of the electrical parameters.

Index Terms—Self-checking checkers, two-rail code checkers, current mode checker, periodic output checkers.

1 Introduction

Modern semiconductor technology applications are characterized by an increased demand for high reliability. Self-Checking Circuits (SCC) [1] are a well-known solution due to their online error detection capability during the normal operation. An SCC consists of a functional circuit (the circuit under monitoring) whose outputs are monitored by a checker. The circuit under monitoring is designed to provide output codewords that belong to an error detecting code, in the fault-free case, and noncodewords in the presence of a fault, with respect to a target fault model. The checker produces an error indication signal whenever the circuit under monitoring produces a noncodeword output. In addition, in case of the checker's internal faults, it must also provide an error indication or it must continue to properly monitor the circuit under monitoring. The above requirements are covered by the Totally Self-Checking (TSC) [2] and the Strongly Code-Disjoint (SCD) [3] properties. A checker is TSC with respect to a set of faults F if it is Self-Testing (ST) and Fault-Secure (FS) for the faults of this set, as well as Code-Disjoint (CD) [1], [2], where:

- A circuit is **ST** for a set of faults F, if, for every fault in F, the circuit produces a noncodeword output for at least one codeword input.
- A circuit is **FS** for a set of faults F, if, for every fault in F, the circuit never produces an incorrect codeword output for all codeword inputs.
- A circuit is **CD** if, for fault-free operation, codeword inputs map into codeword outputs and noncodeword inputs map into noncodeword outputs.

Instead, a circuit is SCD with respect to a set of faults F if, before the occurrence of any fault in F, the circuit is CD and, for every fault in F, either 1) the circuit is ST or 2) the circuit always maps input noncodewords into output noncodewords and, if another fault from F occurs, then either case 1 or 2 is true for the fault sequence.

Any TSC checker is capable of detecting all internal faults if all codewords are available at the checkers' inputs. Unfortunately, in practice, an embedded checker is monitoring a circuit that usually produces a predetermined set of codewords, which may be a subset of the entire code space, and the checker must be testable with this reduced set [4], [5], [6], [7], [8], [9], [10]. However, the design of such a checker is a hard task. A possible design approach is to use additional hardware and/or signals for online generation of all necessary codewords that make a checker TSC with respect to a set of faults [4], [11], [12], but the hardware overhead, the performance degradation, and/or testability problems set up considerable limitations. An alternative way is to apply, offline, the full set of codewords [13]; however, this is not a practical solution in high-reliability real-time applications like space, medicine, avionics, etc.

The special category of the two-rail code (TRC) checkers [1], [2], [4], [5], [6], [7], [8], [14], [15] is frequently used in self-checking applications. TRC checkers are exploited to check the correctness of input words with n pairs of two-railed bits (that is, pairs of bits with complementary values) that compose the codewords. In that case, they are called n-variable TRC (TRC_n) checkers. Usually, n-variable TRC checkers, with $n > 2$, are implemented as a tree of two-variable TRC checkers (e.g., [5]), but their low performance and the required silicon area make them a unattractive solution for today's applications. As an alternative, nontree

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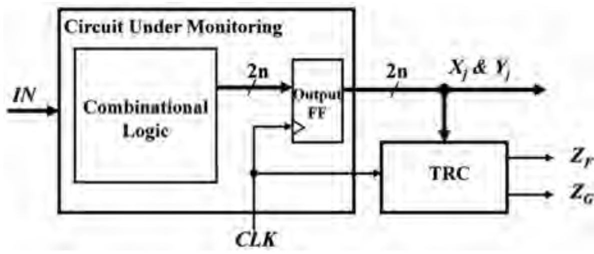

Fig. 1. A self-checking circuit with a TRC checker.

TRC checkers with periodic outputs have been proposed in [13], [16], [17], [18] that are suitable for embedded checker implementations. The outputs of these checkers present alternating complementary values in each clock semiperiod. However, for high n-variable implementations, they also present a considerable degradation in their speed performance and increased requirements in silicon area while, in many cases, stuck-open faults are not covered.

In this paper, we present a fast, parallel, low cost, and periodic output TRC checker that is based on the current mode structure we introduced in [19]. The proposed approach is suitable for the implementation of embedded high fan-in TRC checkers. The new checker is proven to be TSC or SCD for a wide set of realistic faults, while a modified version of it covers transistor stuck-open (TSOP) faults that are not fully detectable in earlier nontree-structured TRC checker designs of the same type [13], [18]. Note that stuck-open faults present a considerable interest in very deep submicron technologies [20], [21], [22]. In addition, as in [13], [16], [17], [18], the checker requires only two input codewords out of a wide variety of equivalent pairs to satisfy the TSC or SCD property for the enhanced set of faults. However, the functional circuit must be capable of providing at least one pair of such codewords.

This paper is organized as follows: In Section 2, the topology and the operation of the proposed TRC checker are analyzed and its CD property is proven. Next, in Section 3, the self-checking property of the circuit with respect to stuck-at (SA), stuck-open, stuck-on, and transient faults is discussed. Design issues and comparisons with the most efficient until now parallel TRC checker proposed in [18] are presented in Section 4. In Section 5, a modified version of the checker, for enhanced testability, is introduced. In Section 6, the self-checking property of the modified circuit with respect to the above fault models is discussed and the bridging fault coverage is also explored. In addition, the design issues are presented and the suitability of the proposed design approach for the implementation of embedded checkers is accentuated. Finally, conclusions are drawn in Section 7.

2 The Proposed Two-Rail Code Checker

The general topology of a circuit that is monitored by a TRC checker is shown in Fig. 1. The circuit under monitoring is designed to produce two-railed output words $(X_j, Y_j, j \in [1, \ldots, n])$ when it is fault-free $(X_j = \overline{Y_j})$ and non-two-railed output words $(X_j = Y_j)$ in case of internal faults. The TRC checker verifies whether the output words of a circuit under monitoring are two-railed or not, providing the two-railed output indication signals Z_F and Z_G.

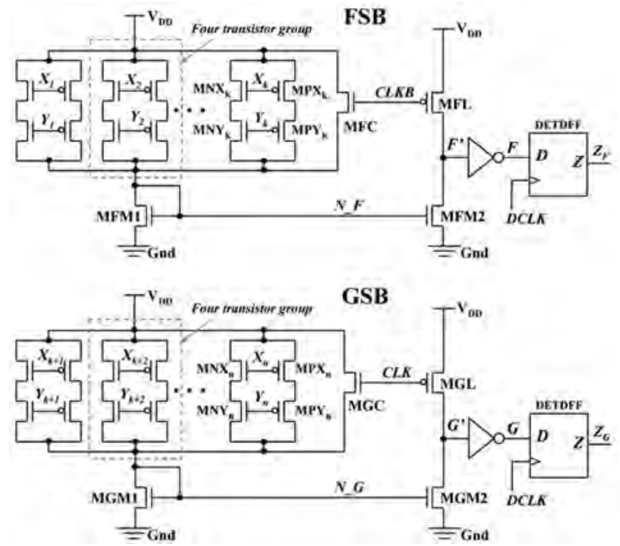

Fig. 2. The proposed two-rail code checker, $k = n/2$.

2.1 Checker Topology

The proposed n-variable TRC checker is presented in Fig. 2. The circuit is divided into two identical subblocks, the F-Subblock (FSB) and the G-Subblock (GSB); it receives n pairs of two-railed inputs $(X_j, Y_j,\ j \in [1, \ldots, n])$ and provides a two-railed pair of outputs Z_F and Z_G, one for each subblock. Since this checker belongs to the periodic output TRC checkers category, it has been designed so that the outputs Z_F and Z_G (and also the pertinent internal nodes of each subblock) present alternating complementary logic values in each semiperiod of the clock signal in order to guarantee that the circuit is TSC with respect to possible SA faults on them. The first subblock is fed by half of the checker input pairs $(X_r, Y_r,\ r \in [1, \ldots, k]$, where $k = n/2)$ and the complementary clock signal *CLKB*, while the second is fed by the rest of the input pairs $(X_s, Y_s,$ $s \in [k+1, k+2, \ldots, n])$ and the clock signal *CLK*. Each pair of inputs (X_j, Y_j) drives two serially connected nMOS transistors (MNX_j and MNY_j) and two serially connected pMOS transistors (MPX_j and MPY_j), as shown in Fig. 2, in the corresponding subblock (a group of four transistors). Thus, there are n-pairs (or $n/2$ groups) of transistors in each block connected in parallel between the V_{DD} power supply and the input terminal (N_F or N_G) of a current mirror in each subblock. A conducting path from V_{DD} to N_F or N_G is formed if a noncodeword is present at the inputs of the checker ($\exists$ at least one j: $X_j = Y_j$).

Additional nMOS transistors, MFC and MGC, are also connected between V_{DD} and the input terminal of the current mirror in each subblock, respectively. The MFC transistor of the FSB is driven by the *CLKB* clock signal, while the MGC transistor of the GSB is driven by the *CLK* clock signal. The two current mirrors are formed by pairs of nMOS transistors, the MFM1-MFM2 for the FSB and the MGM1-MGM2 for the GSB. Moreover, the pMOS transistors MFL and MGL are used as loads at the output terminals F' and G' of the two

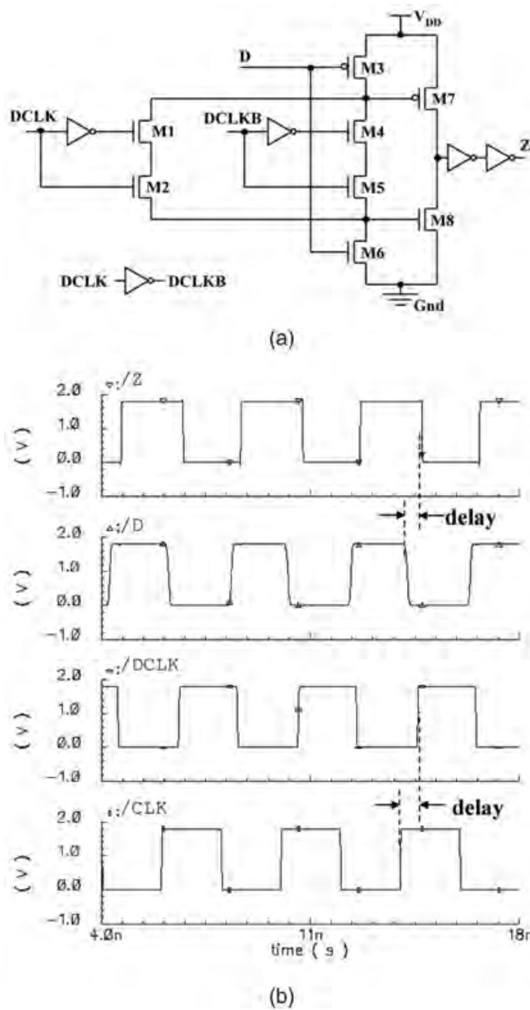

Fig. 3. (a) The double-edge triggered D flip-flop (DETDFF). (b) Signal waveforms.

current mirrors. The MFL transistor is driven by the *CLKB* signal and the MGL by the *CLK* signal. Finally, the responses at nodes F and G are latched, on both clock edges of signal *DCLK*, using two double-edge triggered D flip-flops (DETDFF). The flip-flop is presented in Fig. 3a and is the same as the one proposed in [18]. The DETDFFs provide the two-railed checker outputs Z_F and Z_G. The *DCLK* signal is shown in Fig. 3b and is a copy of the *CLK* signal delayed by a time interval equal to the response delay at the F and G outputs of the checker plus the setup time of the flip-flop.

At the triggering edges of the *DCLK* signal, the checker's nodes F and G always present complementary logic values in the fault-free operation of the circuit under monitoring and noncomplementary in the opposite case. Consequently, the same stands for the final checker outputs Z_F and Z_G that provide the indication of the correct system operation or not, respectively.

2.2 Checker Operation

The checker operation is divided into two phases, transparent to the circuit under monitoring, according to the clock *CLK* semiperiods. Note that the inputs of the checker are supposed to be synchronous. In the fault-free case ($X_j = \overline{Y_j}\ \forall\ j \in [1, \dots, n]$—codeword inputs) and in each phase, the following stand:

- In the first semiperiod, when *CLK* = "1," the parallel pairs of transistors in the FSB and the transistor MFC are in the nonconducting state and, thus, no current passes through the pertinent current mirror, forcing F' to be charged to V_{DD} through MFL, which is in the conducting state. However, the MGC transistor in the GSB is in the conducting state providing current to the input terminal of the corresponding current mirror. Since the MGL transistor is in the nonconducting state, the mirrored current discharges node G' toward Gnd. Consequently, F and G present complementary values ("low" and "high," respectively) at the end of the first semiperiod of the clock.
- In the second semiperiod, when *CLK* = "0,", the MFC transistor in the FSB is in the conducting state, providing current to the input terminal of the corresponding current mirror. Since the MFL transistor is in the nonconducting state, node F' is discharged toward Gnd. On the contrary, the parallel pairs of transistors in the GSB and the transistor MGC are in the nonconducting state and, thus, no current passes through the pertinent current mirror forcing G' to be charged to V_{DD} through MGL, which is in the conducting state. The result is F and G also present complementary values ("high" and "low," respectively) at the end of the second semiperiod of the clock.

Thus, in the fault-free case, the pairs of nodes F and G as well as Z_F and Z_G are always in complementary states (two-railed) at the end of each clock semiperiod.

In case a non-two-rail word is present at the inputs of the checker, at least one or more input pairs (X_j, Y_j) have equal values ($X_j = Y_j$—noncodeword inputs). The following three cases are observed:

1. the non-two-rail input pairs feed only the FSB,
2. the non-two-rail input pairs feed only the GSB, and
3. there are some non-two-rail pairs that feed the FSB and others that feed the GSB.

In case 1, there is at least one pair of serially connected transistors in FSB, driven by the non-two-rail input pair that will be in the conducting state (either a pMOS pair when $X_j = Y_j =$ "0" or an nMOS pair when $X_j = Y_j =$ "1"). Thus, in the first semiperiod of the clock, there will be a current flow through the current mirror of the FSB that will discharge (or keep discharged) node F' since the current mirror is designed to be more conductive (dominant) over the load transistor MFL. Consequently, the F node turns "high" and, since the GSB response does not depend on the input values during the first semiperiod, both F and G will be in the "high" state.

Similarly, in case 2, there will be at least one pair of serially connected transistors in GSB that is driven by the non-two-rail input pair and, thus, it is in the conducting state. As a result, in the second semiperiod of the clock, there will be a current flow through the current mirror of the GSB that will discharge (or keep discharged) node G' since this current mirror is also designed to be more

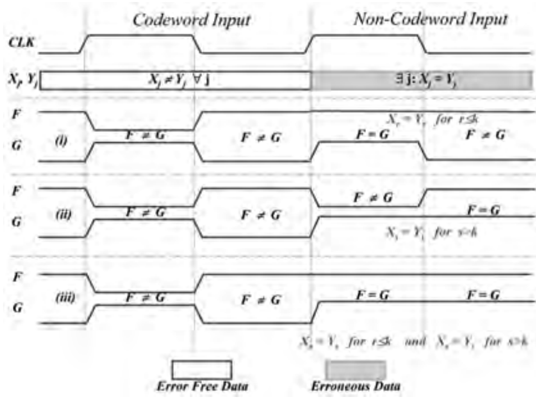

Fig. 4. Checker's response under codeword and noncodeword inputs.

conductive (dominant) over the load transistor MGL. Consequently, the G node turns "high" and, since the FSB response does not depend on the input values during the second semiperiod, both F and G will be in the "high" state.

Finally, in case 3, an erroneous pair of inputs affects both FSB and GSB. Consequently, according to cases 1 and 2, F and G will be in the "high" state in both semiperiods of the clock.

The waveforms in Fig. 4 show the response of the checker's nodes F and G in the presence of codeword inputs and all possible noncodeword input conditions discussed above. In all three cases, the Z_F and Z_G outputs of the checker will capture the responses on F and G, indicating the presence or absence of errors. From the above analysis, it is proven that the proposed circuit is CD since codeword inputs map into codeword outputs and noncodeword inputs map into noncodeword outputs.

3 The Self-Checking Property

In this section, the self-checking property of the proposed checker is discussed with respect to a set of faults consisting of

1. line SA faults,
2. transistor stuck-on faults,
3. transistor stuck-open faults, and
4. transient faults.

The following two common assumptions in the checker's design [5], [18], [23] have been taken into account: 1) A single fault occurs at a time and 2) the time between two successive faults is enough to permit the application of all possible codewords (or at least the required ones).

3.1 Line Stuck-At Faults

We can observe five cases of possible line SA faults:

1. on the input lines of the checker X_j, Y_j, $j \in [1, \ldots, n]$,
2. on the checker lines F, G, Z_F, and Z_G,
3. on the internal lines of the checker N_F, F', N_G, and G',
4. on the *CLK* or *CLKB* clock signal lines, and
5. on the internal lines of the DETDFFs.

These are analyzed as follows:

1. SA faults on the input lines X_j, Y_j, $j \in [1, \ldots, n]$, of the checker are equivalent to non-two-rail words on them. Therefore, the checker is TSC with respect to these faults.
2. Obviously, the checker is TSC considering SA faults on lines F, G, Z_F, and Z_G.
3. An SA "0" or "1" fault on N_F (N_G) is equivalent to an SA "0" or "1" fault on the F (G) line of the checker. Similarly, an SA "0" or "1" fault on F' (G') is equivalent to an SA "1" or "0" on line F (G). Consequently, according to item 2, the checker is TSC for this kind of fault.
4. An SA "0" fault on *CLK* (*CLKB*) is equivalent to an SA "0" on line G (F). Moreover, an SA "1" fault on *CLK* (*CLKB*) is equivalent to an SA "1" fault on line G (F). Thus, the checker is TSC with respect to these faults.
5. The used DETDFFs are identical to the pertinent output flip-flops in [18] and the same stands for their input signal conditions. Since it has been proven in [18] that these faults are detectable, the checker is TSC for this kind of fault.

3.2 Transistor Stuck-Open Faults

TSOP faults can be categorized into five groups as follows: those affecting

1. the transistors that are driven by the checker inputs (X_j, Y_j, $j \in [1, \ldots, n]$),
2. the transistors that are driven by the clock signals *CLK* and *CLKB*,
3. the transistors of the current mirrors,
4. the transistors of the inverters, and
5. the transistors of the DETDFFs.

The above cases are analyzed as follows:

1. The TSOP faults of the first kind are not sensitized by input codewords and, thus, they are not detectable. Consequently, the checker is not ST with respect to these faults but remains FS. In addition, there are also noncodeword inputs that are not detectable by the checker in the presence of this kind of fault. Note that the periodic output TRC checker presented in [18] is also non-ST as is the proposed one for the same number and type of transistors (those driven by the checker inputs). As was proposed in [18], it could be possible to detect these faults offline by applying the proper non-two-rail words. The necessary non-two-rail words are those where $(X_i, Y_i) = (\text{"1"}, \text{"1"})$ and then ("0," "0"), while $\forall\, j \neq i$, it stands that $(X_j, Y_j) = (0, 1)$ or (1, 0), with $i, j \in [1, \ldots, n]$. Another approach is to use an additional BIST structure to detect these faults, as is recommended in [24]. We will present in Section 5 a modified version of our checker with enhanced fault coverage that is capable of detecting this kind of faults.
2. In the case of a TSOP fault that affects the MFC (MGC) transistor of the FSB (GSB), it will result in a "low" response at the F (G) line of the checker during the second (first) semiperiod of the clock.

Thus, this fault is detectable. The same stands when the transistor MFL (MGL) is affected by a TSOP fault. The line F (G) of the checker is "high" during the first (second) semiperiod and, thus, the fault is detectable. Consequently, the checker is TSC with respect to these faults.

3. A TSOP fault in the MFM1 (MGM1) transistor will lead node N_F (N_G) to be permanently charged to $V_{\rm DD}$. Thus, transistor MFM2 (MGM2) will always be in the conducting state, turning F (G) to "high" during the first (second) semiperiod of the clock. Consequently, the checker is TSC for this fault. Moreover, a TSOP fault on MFM2 (MGM2) will result in a "low" value at the F (G) line of the checker during the second (first) semiperiod of the clock. Hence, the checker is also TSC for this fault.
4. A TSOP fault at the pMOS transistor of the inverter is equivalent to an SA "0" fault at its output, while a TSOP fault at the nMOS transistor is equivalent to an SA "1" fault at its output. Thus, according to item 2 in Section 3.1, the checker is TSC for these faults.
5. Finally, TSOP faults that affect the transistors of the DETDFFs have been proven in [18] to be detectable and the checker is TSC with respect to them.

3.3 Transistor Stuck-On Faults

Similarly to the TSOP faults, transistor stuck-on (TSON) faults can be categorized into five groups as follows: those affecting

1. the transistors that are driven by the checker inputs ($X_j, Y_j, j \in [1, \ldots, n]$),
2. the transistors that are driven by the clock signals *CLK* and *CLKB*,
3. the transistors of the current mirrors,
4. the transistors of the inverters, and
5. the transistors of the DETDFFs.

The above cases are analyzed as follows:

1. A TSON fault on a transistor of the FSB (GSB) that is driven by the checker inputs X_j or Y_j, $j \in [1, \ldots, n]$, is detectable since there exists an input codeword with $(X_j, Y_j) = (0, 1)$ or $(1,\ 0)$, respectively, to sensitize it. This means that, in the fault-free case, the corresponding transistor is in the nonconducting state while the other transistor in the pair is in the conducting state. However, in the faulty case, both transistors are conducting. Thus, after the application of this codeword at the checker inputs, there will be a current flow through the current mirror of the FSB (GSB), which will set node F' (G') to "low" during the first (second) semiperiod of the clock since the current mirror is dominant over the load transistor MFL (MGL). Thus, node F (G) will be to a "high" state during this semiperiod and the fault will be detected. Consequently, the checker is TSC for this kind of fault.
2. A TSON fault that affects the MFC (MGC) transistor of the FSB (GSB) will result, as in case 1, in a "high" response at the F (G) output of the checker during the first (second) semiperiod of the clock. Thus, this fault is detectable and the checker is TSC with respect to this fault. However, a TSON fault on the MFL (MGL) transistor will either lead the output F (G) to "low" at the second (first) period of the clock or does not affect the checker's logic behavior. Hence, concerning this fault, the checker is either TSC or SCD.
3. The presence of a TSON fault on transistor MFM1 (MGM1) will prohibit any current flow through the right branch of the current mirror, that is, transistor MFM2 (MGM2), resulting in a "low" value on the F (G) output of the checker during the second (first) semiperiod of the clock. Thus, this kind of fault is detectable and the checker is TSC with respect to this fault. Moreover, a TSON fault on transistor MFM2 (MGM2) will lead to a "high" value at the output F (G) of the checker during the first (second) semiperiod of the clock. Therefore, the checker is TSC for a TSON fault on transistor MFM2 (MGM2).
4. A TSON fault on the pMOS (nMOS) transistor of the inverter will either lead the output F or G to a value that will be treated as "low" ("high") by the corresponding flip-flop or will not affect the checkers' logic behavior. Consequently, the checker is either TSC or SCD for these faults.
5. Finally, TSON faults that affect the transistors of DETDFFs have been proven in [18] to be detectable and the checker is TSC with respect to them.

3.4 Transient Faults

Considering possible transient faults, for instance due to a single event transient in a checker's node, two cases exist. First, the transient pulse is attenuated in the internal nodes of the checker without affecting node F (or G) or the pulse is not latched by the triggering edge of the delayed clock *DCLK* at the DETDFFs and, thus, the checker satisfies the SCD property. Second, the effect of the pulse is propagated to the node F or G (only one node is affected since the two subblocks are independent) and is latched at the corresponding DETDFF, where it will be detected, and the checker is TSC for this fault.

4 Design Issues and Simulation Results

The proposed parallel TRC checker has been designed in the standard 0.18μm CMOS technology of ST Microelectronics for a variety of n-variable values ranging from 8 to 512. The used power supply was 1.8 V. The operation of our checker has been verified by electrical simulations in a full range of Process, Voltage, Temperature (PVT) conditions, that is, 1) the process corners for the used technology provided by ST, 2) power supply variations up to ± 10 percent, and 3) temperature variations from 0°C to 125°C.

Independently of the n-variable value in these designs, the sizes of the used transistors (excluding the four transistors of the current mirrors) were fixed and their W/L values are shown in Table 1.

The sizes of the two transistors MFM1-MFM2 and MGM1-MGM2 in each current mirror depend on the value

TABLE 1
Transistor Sizes W/L in μm

FSB and GSB Transistor Sizes - Excluding the Current Mirrors										
					DETD Flip-Flop					
MPX_i MPY_i	MNX_i MNY_i MFC MGC	MFL, MFG	Mirror Inverter pMOS	Mirror Inverter nMOS	M1, M2 M4, M5	M3 M7	M6	M8	Inverter pMOS	Inverter nMOS
0.5 / 0.18	0.28 / 0.18	0.5 / 0.8	1.24 / 0.18	0.7/ 0.18	1.1 / 0.26	1.54/ 0.18	0.46 / 0.18	1.02 / 0.18	0.56 / 0.18	0.28 / 0.18

TABLE 2
Transistor Sizes for the Current Mirrors

n-variable	8	16	32	64	128	256	512
Width (μm) [MFM1(MGM1) – MFM2(MGM2)]	0.6 – 2.8	1.0 – 3.5	1.9 – 4.5	3.0 – 6.2	4.0 – 9.0	4.7 – 12.0	5.0 – 14.0

TABLE 3
Comparisons with Respect to 1) Silicon Area, 2) Response Delay Time, and 3) Power Consumption

	Silicon Area Cost (UST)			Response Delay (ps)			Power Consumption (μW)		
Fan-In - n -	Proposed	[18]	Reduction	Proposed	[18]	Reduction	Proposed	[18]	Reduction
8	187	252	25,8%	298	355	16,1%	64	21.3	-200,5%
16	239	415	42,4%	328	505	35,0%	95	27.7	-243,0%
32	342	776	55,9%	375	775	51,6%	109	40	-172,5%
64	540	2324	76,8%	408	1205	66,1%	119	87.1	-36,6%
128	924	7925	88,3%	517	1845	72,0%	136	245	44,5%
256	1663	34965	95,2%	695	3097	77,6%	174	976	82,2%
512	3106	135675	97,7%	1055	4965	78,8%	215	3840	94,4%

of the n-variable and their widths (W) for various n-values are presented in Table 2 $(L = 0.18\mu\text{m})$.

From the above discussion, it is obvious that we can easily exploit automatic physical design (layout) generators like those commonly used in memory design for the construction of the required checker using a simple and small library of leaf cells consisting of a couple of transistor pairs (pMOS and nMOS), an MFC (MGC)-sized transistor, an MFL (MGL)-sized transistor, a NOT gate, a DETDFF, and few various sizes current mirrors with the corresponding load transistors. In Section 6.5, we will provide more details on this ability.

The operation of the proposed TRC checker has been verified for the fault-free and all of the possible faulty conditions in the checker according to the fault models discussed in Section 3, as well as for all possible types of codeword and noncodeword inputs.

For comparison reasons, the checker presented in [18] has also been designed for the same range of n-variable alternatives. Both checkers have been optimized with respect to their response time in order to provide the minimum response delay in each case. Moreover, both checkers have been designed to be functional for the full range of PVT conditions. In Table 3, design issues and simulation results are presented for both circuits. Initially, in columns 2 and 3, the implementation cost in unit size transistors (USTs) for each design is presented. As the implementation cost in UST, we define the number of minimum size transistors according to the technology used that will occupy the same area as the actual transistors in the design. Furthermore, in column 4, the cost reduction of our topology over the one in [18] is given. Next, comparisons based on simulation results between the two checkers are presented. The worst-case response time (columns 5 and 6) and the power consumption in the fault-free case (columns 8 and 9) are shown. The corresponding reductions are provided in columns 7 and 10, respectively. According to Table 3, the proposed checker in this work is superior to that of the checker in [18] with respect to the required silicon area and the response delay time, especially for high values of the n-variable. In addition, for high n-variable values, the new checker also turns out to be more power efficient over the previous approach.

A graphical presentation of the response delays for the two checkers is illustrated in Fig. 5. The speed performance of the proposed checker originates from the current mode operation. The adopted current mirror topology is capable of providing fast sensing of the current flow through the array of the parallel-connected pairs of transistors without the need for a full voltage swing on the high parasitic capacitance nodes, N_F and N_G, of the checker, as in the pertinent nodes in [18]. This way, fast response times can be achieved with low silicon requirements, especially in the case of high n-variable values. The only requirement is to provide a quite low current as input to the current mirrors of the checker. Moreover, the reduced voltage swing on these nodes provides power savings in the case of large parasitic capacitances on these nodes (high n-variable

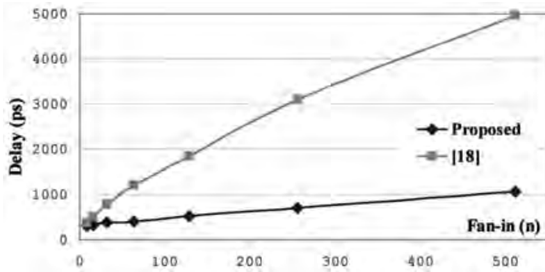

Fig. 5. Delay comparisons with respect to the fan-in (n).

values) despite the DC current path in each subblock during the pertinent semiperiod.

Note that the downscaling of the power supply voltage in future technologies is not expected to affect the speed performance characteristics of the proposed TRC checker. Recent reports on CMOS technology evolution [25] assert that it will be feasible to maintain, from generation to generation, a 25 percent increase in transistors' drive current, at the same subthreshold leakage, using high-k and metal gate devices. Consequently, the driving capability of the input transistors in the proposed design will be adequate to support high-speed TRC checker implementations.

Finally, considering the noise sensitivity of the checker, we should mention that its inputs are digital signals (full swing signals and not small analog signals) that are characterized by precisely defined noise margins. Since the checker does not need to detect small signal variations at its inputs, it is inherently immune to the input noise.

5 Modified Version of the Checker for Enhanced Testability

In order to extend the self-checking property of the circuit to the uncovered TSOP faults, a modified version is presented in Fig. 6. In the previous version of the checker (Fig. 2), each of the two input signals X_j and Y_j drives a pair of serially connected pMOS and a pair of serially connected nMOS transistors. These four transistors form a group. In the new circuit, there is a fifth nMOS transistor in the group that is controlled by a select signal S_j. That fifth nMOS transistor "connects" the two pairs, as shown in Fig. 6, and is used to enhance the testability of the group. The added transistors replace the MFC and MGC transistors in Fig. 2 as well as their operation in the two subblocks.

The select signals S_j ($j \in [1, \ldots, n]$) are generated by a Cyclic Shift Register (CSR) of $k = n/2$ bits and a NOR gate array, as shown in Fig. 7. The CSR is preset to a pattern that has only 1 bit position with the "0" value. When *CLK* = "0," then $S_j =$ "0" ($j \in [1, \ldots, n]$) except for only one S_r signal ($r \in [1, \ldots, k]$) that has the "1" value which is related to the r-bit position in the CSR with the "0" value. In symmetry, when *CLK* = "1," then $S_j =$ "0" ($j \in [1, \ldots, n]$) except for only one S_{k+r} signal ($r \in [1, \ldots, k]$) that has the "1" value, which is related to the r-bit position in the CSR with the "0" value.

Note that, in the case where n is odd, then $k = \lceil n/2 \rceil$ and an additional (dummy) group must be inserted in the GSB block with the X and Y inputs driven by stable complementary values.

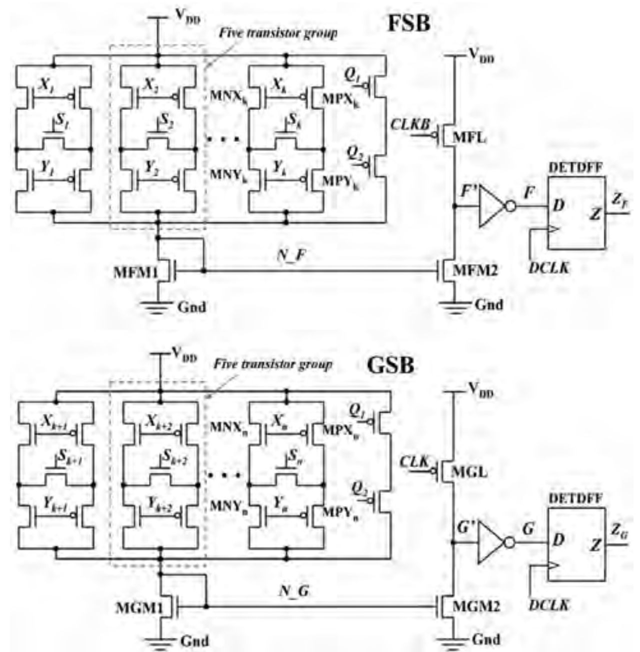

Fig. 6. The modified two-rail checker, $k = n/2$.

The checker's output nodes Z_F and Z_G always present complementary logic values in the fault-free case and noncomplementary in the opposite case providing the indication of the correct system operation or not. As earlier, the checker operation is divided into two phases, transparent to the circuit under monitoring, according to the clock *CLK* semiperiods. In the fault-free case ($X_j = \overline{Y_j}\ \forall\ j \in [1, \ldots, n]$) and for each phase, the following stand:

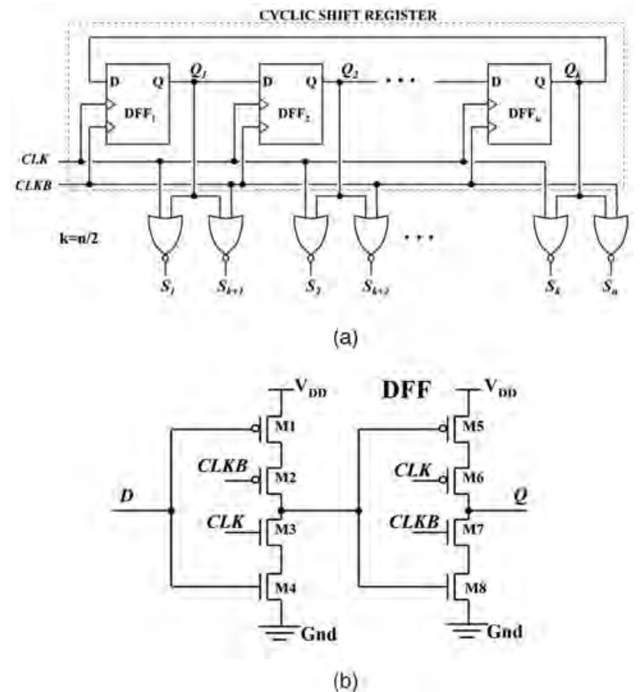

Fig. 7. (a) Select signal generation circuitry, $k = n/2$. (b) The D flip-flop.

1. In the first semiperiod, when *CLK* = "1," each pair of transistors driven by the inputs $(X_j, Y_j, j \in [1, \ldots, n])$ has one transistor in the nonconducting state and one transistor in the conducting state. Moreover, all transistors in the FSB driven by the S_j signals $(j \leq k)$ are in the nonconducting state. Thus, no current passes through the pertinent current mirror of FSB forcing F' to be charged to V_{DD} through MFL that is in the conducting state. However, there is a single transistor in the GSB, driven by the S_{k+r} signal $(r \in [1, \ldots, k])$, that is in the conducting state $(S_{k+r} = \text{"1"})$. Thus, there will be a current path from V_{DD} to the input terminal (N_G) of the corresponding current mirror through this transistor and the two conducting transistors, a pMOS and an nMOS transistor, of the pertinent pairs depending on the input combination (X_{k+r}, Y_{k+r}). No other current path is formed. Since the MGL transistor is in the nonconducting state, the mirrored current that is generated discharges node G' toward Gnd. Consequently, F and G present complementary values ("0" and "1," respectively) in the first semiperiod of the clock and the same for Z_F and Z_G after the triggering edge of the *DCLK* clock signal.
2. Similarly, in the second semiperiod when *CLK* = "0," the opposite case stands, also setting Z_F and Z_G to complementary values "1" and "0," respectively.

Thus, in the fault-free case, nodes Z_F and Z_G are always in complementary states (two-railed).

In the case where one or more non-two-rail words are present at the inputs of the checker, the circuit operation is exactly the same as that of its earlier version in Section 2 (see Fig. 4): 1) If the non-two-rail input pairs only feed the FSB, then both F and G will be in the "1" state during the first semiperiod of the clock *CLK*; 2) if the non-two-rail input pairs only feed the GSB, then both F and G will be in the "1" state during the second semiperiod; and 3) if there are some non-two-rail pairs that feed the FSB and the rest feed the GSB, then F and G will be in the "1" state in both semiperiods of the clock. After the triggering edges of the *DCLK* signal, the Z_F and Z_G outputs of the checker will capture the responses on F and G, indicating the presence of the error(s).

From the above analysis, it is obvious that the circuit is code-disjoint.

6 The Self-Checking Property and Design Issues of the Modified Checker

Initially, the self-checking property of the modified checker is discussed in this section with respect to the same set of faults as in its previous version. With the goal that the circuit meets the self-checking property in the presence of CSR, we have inserted a pair of serially connected pMOS transistors in both the FSB and the GSB subblocks that are driven directly by any two successive stage outputs of the CSR (e.g., Q_1 and Q_2), as shown in Fig. 6. In the fault-free case of CSR, at least one of the pMOS transistors in each pair is in the nonconducting state and the operation of the checker is not affected.

6.1 Line Stuck-at Faults

Possible line SA faults of the following categories:

1. on the input lines of the checker X_j, Y_j, $(j \in [1, \ldots, n])$,
2. on the lines F, G, Z_F, and Z_G,
3. on the internal lines of the checker N_F, F', N_G, and G', and
4. on the internal lines of the DETDFFs,

are identical to the pertinent cases in Section 3.1 and the checker is TSC with respect to these faults. In addition:

5. An SA "0" on a select signal S_j will result in no current path formation in the corresponding subblock FSB (GSB) during the second (first) semiperiod when S_j must be "1." Thus, both F and G will be "0" during this semiperiod. An SA "1" on a select signal S_j will result in a current path formation during the first (second) semiperiod, where no conducting path should exist in the FSB (GSB). Consequently, both F and G will be "1" during this semiperiod. Therefore, the checker is TSC with respect to these faults.
6. An SA "1" at an output Q_r $(r \in [1, \ldots, k])$ of a flip-flop in the CSR (or, equivalently, the pertinent input of a NOR gate) will result in an all "1" state of the CSR after at most k clock cycles. In that case, no select signal S_j can be activated, resulting in "0" responses in both F and G. Similarly, an SA "0" fault on these lines will result in an all "0" state of the CSR after at most k clock cycles. In that case, both pairs of pMOS transistors driven by Q_1 and Q_2 in the FSB and GSB subblocks will be in a conducting state for a whole clock period. Thus, both F and G will be "1." The checker is TSC for this kind of faults.
7. An SA "1" fault at the *CLK* (*CLKB*) lines is equivalent to an SA "1" fault on line G (F) (since the clock signals drive the load transistors MGL and MFL, respectively) and the circuit is TSC with respect to this fault. An SA "0" fault at *CLK* (*CLKB*) is equivalent to an SA "1" ("0") fault at the Q_r $(r \in [1, \ldots, k])$ outputs of the D flip-flop (DFF) (Fig. 7b). Moreover, since the clocked input of all NOR gates that provide the signals S_r (S_{k+r}) $(\forall r \in [1, \ldots, k])$ is at SA "0," the output signals S_r (S_{k+r}) will be permanently at the "0" ("1") state and the case is equivalent to case 5. Consequently, the circuit is TSC for this fault.

6.2 TSOP Faults

TSOP faults are analyzed as follows:

1. A TSOP fault on a transistor of the FSB (GSB) that is driven by a checker input X_j or Y_j is detectable since there exists an input codeword with $(X_j, Y_j) = (0, 1)$ or (1, 0), respectively, to sensitize it. In the presence of the fault and after the application of this codeword at the checker inputs, no current path can be formed in the FSB (GSB) during the second (first) semiperiod and during the time frame when S_j is "1," although the transistor under test should

be in a conducting state according to its gate value. In that case, both F and G will be "0" during this semiperiod and, consequently, the checker is TSC with respect to these faults.

The cases of TSOP faults

2. on the transistors of the FSB or GSB that are driven by the *CLK* and *CLKB* signals,
3. on the transistors of the current mirrors,
4. on the transistors of the inverters, and
5. on the transistors of the DETDFFs

are identical to the pertinent cases in Section 3.2 so that the checker is TSC with respect to these kinds of faults.

6. A TSOP fault on a transistor that is driven by a select signal S_j will result in no current path formation in the corresponding subblock FSB (GSB) during the second (first) semiperiod when S_j is "1." Thus, both F and G will be "0" during this semiperiod and the checker is TSC with respect to these faults.
7. A TSOP fault on transistor M1 or M2 or M7 or M8 in a DFF of the CSR will result in a permanent "1" value on its output. Consequently, the CSR turns to the all "1" state after at most k clock cycles and this case is equivalent to that in case 6 in Section 6.1.
8. A TSOP fault on M3 or M4 or M5 or M6 in a DFF of the CSR will result in a permanent "0" value on its output. Consequently, the CSR turns to the all "0" state after at most k clock cycles and this case is equivalent to that in case 6 in Section 6.1.
9. A TSOP fault on a pMOS transistor of a NOR gate will result in a permanent "0" value at the gate output after its first discharge. This case is equivalent to case 5 in Section 6.1. Moreover, a TSOP fault on the nMOS transistor of a NOR gate that is driven by the clock signal will result in a permanent "1" value at the gate output during a whole clock period when the output of the corresponding DFF that drives this NOR gate is "0." This case is also equivalent to case 5 in Section 6.1.
10. A TSOP fault on the nMOS transistor of a NOR gate that is driven by the output of the corresponding DFF will never affect the circuit operation since this transistor is redundant. This is due to the fact that the "00" input state of the NOR gate is always followed by the state where at least the clocked input turns to "1." Thus, the gate output is discharged and remains discharged in the subsequent semiperiod when the clocked input turns to "0" (memory state), as it is the case in the fault-free operation since the DFF output is "1." A subsequent TSOP fault on the nMOS transistor that is driven by the clocked input will result in a permanent "1" value at the output of the NOR gate and this case is equivalent to case 5 in Section 6.1.

Thus, the circuit is TSC with respect to the faults of classes 1 to 9 and SCD for class 10.

11. A TSOP fault on a transistor of the FSB or GSB that is driven either by the Q_1 or Q_2 signal is not detectable. One way is to test these transistors offline just after the system power up. In that case, a pattern with two successive "0" states is inserted in the CSR. When Q_1 and Q_2 are both "0," then, in the fault-free case, the outputs F and G are both "1"; in, the other case, a TSOP fault is detected. However, note that one of the two pairs is redundant, which reduces the probability that such a fault will alter the circuit operation. Moreover, the checker remains FS in the presence of these faults.

6.3 Transistor Stuck-on Faults

Similarly to the TSOP faults, TSON faults are analyzed as follows:

The cases of TSON faults

1. on the transistors that are driven by the checker inputs $(X_j, Y_j, j \in [1, \dots, n])$,
2. on the transistors of the current mirrors,
3. on the transistors of the two inverters and the DETDFFs

are identical to the corresponding faults in Section 3.3 and the checker is either TSC or SCD for them.

4. A TSON fault on the MFL (MGL) transistor does not affect the checker's logical behavior but increases the power consumption. Concerning this fault, it is proven that the checker is SCD.
5. A TSON fault on a transistor that is driven by a select signal S_j will result in a current path formation in the corresponding subblock FSB (GSB) during the first (second) semiperiod. Both nodes F and G will be "1" during this semiperiod and, thus, the checker is TSC for this kind of faults.
6. A TSON fault on transistor M1 or M8 in a DFF of the CSR will result either in successive "0" responses of the cell or it will not have an effect on the circuit operation, depending on the transistor strength. In the first case, as in case 6 in Section 6.1, after at most k clock cycles, both of the two pairs of pMOS transistors driven by Q_1 and Q_2 in the FSB and GSB subblocks will be in a conducting state for a whole clock period. Thus, both F and G will be "1" and the circuit is TSC. In the second case, it is proven that the circuit is SCD.
7. A TSON fault on the transistor M2 or M7 in a DFF of the CSR will result in a sequence of "0" responses of the cell and, according to the previous case (item 6), the circuit is TSC.
8. A TSON fault on transistor M4 or M5 in a DFF of the CSR will result either in the deletion of the "0" state from the register or it will not have any effect on the circuit operation, depending on the transistor strength. In the first case, as in case 5 in Section 6.1, no select signal S_j can be activated, resulting in "0" responses in both F and G, and the circuit is TSC. In the second case, it is proven that the circuit is SCD.
9. A TSON fault on transistor M3 or M6 in a DFF of the CSR will result in the deletion of the "0" state from the register and, according to the previous case (item 8), the circuit is TSC.
10. For the NOR gates, the decision is to make the nMOS transistors dominant (more conductive) over the pMOS transistors. This way, a TSON fault on a pMOS

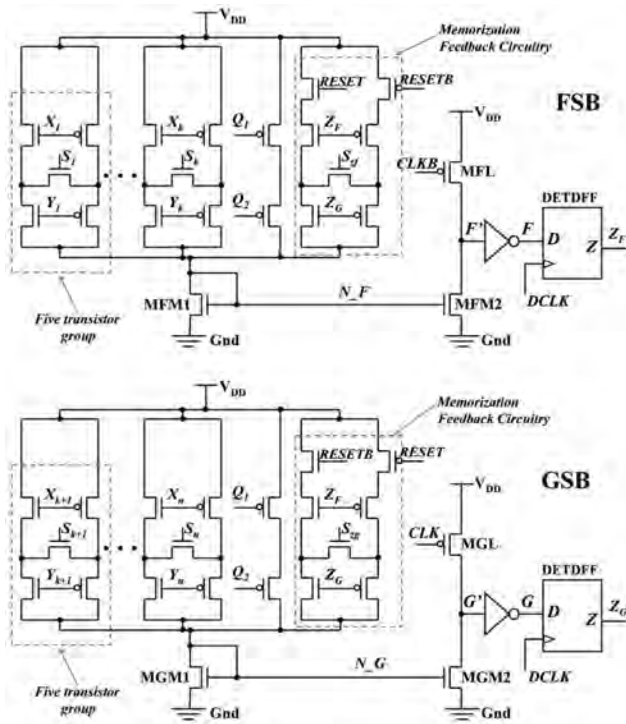

Fig. 8. The complete checker design.

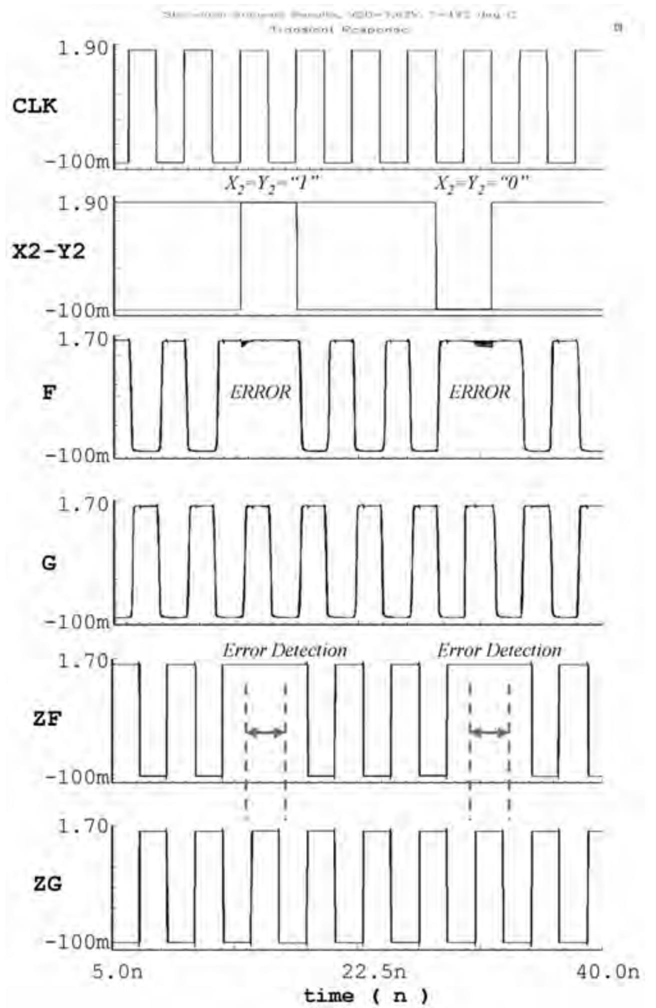

Fig. 9. Monte Carlo analysis waveforms for $n = 64$ with $V_{DD} = 1.62V$ and $T = 125°C$.

transistor does not affect the circuit operation and the circuit is SCD with respect to this fault. However, a TSON fault on an nMOS transistor will result in a permanent "0" response of the gate and, thus, according to case 5 in Section 6.1, the circuit is TSC.

11. A TSON fault on a transistor that is driven by the Q_1 or Q_2 signal in the FSB or GSB blocks will result in a conducting state of the pair for a whole clock period when the other transistor will take the "0" value on its gate. Thus, this fault is equivalent to the faults in case 5 and the checker is TSC for it.

6.4 Transient Faults

Possible transient faults in the modified version of the checker are covered as in its earlier version (see Section 3.4), except for those transient faults in the CSR that turn the output of a DFF flip-flop from "1" to "0," and this erroneous value is captured in the next triggering edge of the clock by the subsequent flip-flop. To confront with this situation, we have decided to reset the CSR at the end of each complete shifting cycle (that is equal to $k = n/2$ clock periods). This way, the error is corrected without any problems in the checker operation since the time period of k clock cycles is too small compared to the time between two successive faults, according to the two common

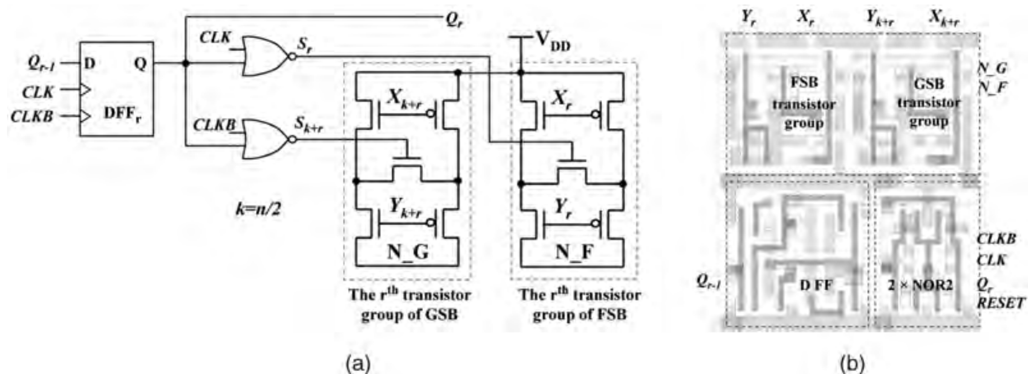

Fig. 10. The basic cell. (a) Schematic. (b) Layout.

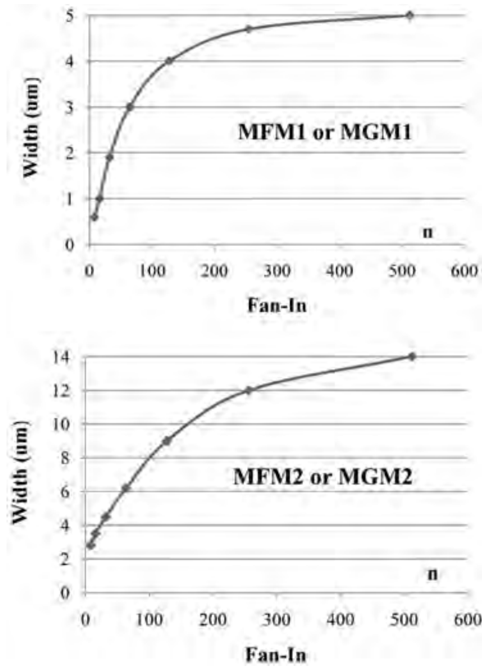

Fig. 11. The current mirrors' transistor widths for various n-variable values.

assumptions in the checkers' design that we have mentioned at the beginning of Section 3.

Finally, in order to provide the checker with the ability to memorize the error indication responses on the outputs Z_F and Z_G, the feedback technique, proposed in [26], can be exploited as shown in Fig. 8. The *RESET* signal is initially set to "1." In the fault-free case, the outputs Z_F and Z_G have complementary values. So, the feedback mechanism does not interfere with the checker operation since at least one of the three serially connected pMOS or nMOS transistors is in the nonconducting state. In case of an error detection, Z_F and Z_G present equal values (either "0" or "1") so the corresponding triplet of serially connected transistors (pMOS or nMOS, respectively) is set in the conducting state in both FSB and GSB, forcing F and G permanently into the "high" state until the *RESET* signal is set to "0" for at least one clock period. In order to obtain the self-checking property of the "memorization" feedback circuitry, with respect to the TSOP faults, an extra stage must be added to the CSR to generate the S_{zf} and S_{zg} control signals in Fig. 8.

6.5 Modified Checker Design and Simulation Results

The modified version of the proposed parallel TRC checker has also been designed in the same 0.18μm CMOS technology ($V_{DD} = 1.8$ V) for a variety of n-variable values ranging from 8 to 512. Again, the operation of the checker has been verified by electrical simulations in a full range of PVT conditions for the fault-free and all the possible faulty conditions in the checker according to the fault models discussed in Section 6, as well as for all possible types of codeword and noncodeword inputs. Moreover, Monte Carlo mismatch analysis has been performed using the statistical models of our technology that cover all process parameters. Indicatively, simulated waveforms are shown in Fig. 9.

With the goal of illustrating the ability to exploit automatic layout generators in the design of the proposed checker, layout views of the various leaf cells that compose the checker have been implemented. The first cell, the basic cell of the checker, is shown in Fig. 10 and its size is independent of the n-variable. It consists of one DFF from the CSR and the corresponding two NOR gates, plus two groups of transistors, one for the FSB and one for the GSB. The basic cell is repeated to form the FSB, the GSB, and the CSR. The layout of the basic cell is shown in Fig. 10b. The second cell is the NOT gate and the DETDFF for which the size is also independent of the n-variable. Finally, the third cell is the current mirror and its load transistor. The size of this cell varies with the n-variable; however, for a range of n-variable values, we can use the same cell, keeping the number of its different versions very small (less than 10).

Fig. 11 shows the relationship between the transistors' widths in the two current mirror pairs and the value of the n-variable. The corresponding curves are obtained by simulations (parametric analysis) aiming to optimize the checker for high-speed operation. According to Fig. 11, the values of the transistor widths come to saturation as the n-variable increases. Table 4 presents a possible width assignment for the current mirror transistors, which provides a good trade-off between the number of the current mirror leaf cells in the library and the checker's speed.

In Fig. 12, the layout view of the modified version of the checker is given for $n = 64$, where the folding design approach, commonly used in memories, has been adopted for the basic cells.

The modified version of the proposed parallel TRC checker requires two to five times more silicon area, it is from 49 percent to 66 percent slower, and it consumes from 4 percent to 34 percent more power with respect to its original version for the range of n-variable values under consideration. However, it is capable of covering all TSOP faults in it in the case where this is imperative for the design [21], [22]. Note that the parallel TRC checker presented earlier in [18] does not provide full coverage of the TSOP faults.

TABLE 4
Transistor Width Assignment for the Current Mirrors' Leaf Cells for Various n-Values

n-variable	4 – 12	13 – 22	23 – 42	43 – 86	87 – 172	173 – 340	341 – 684
Width (µm) (MFM1(MGM1) & MFM2(MGM2))	0.6 & 2.8	1.0 & 3.5	1.9 & 4.5	3.0 & 6.2	4.0 & 9.0	4.7 & 12.0	5.0 & 14.0

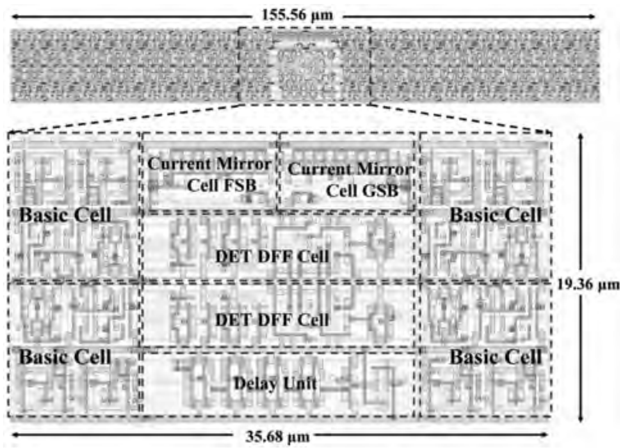

Fig. 12. Layout of the TRC checker for $\mathrm{n} = 64$.

6.6 Resistive Bridging Faults

In order to validate the ability of the checker to detect bridging faults, extensive simulations (for all possible faults of this kind) have been carried out considering the case of $n = 64$ and using the extracted circuit netlist from the layout design of the checker. In this study, bridging faults between adjacent nodes in the same physical layer are taken into account.

Let us initially consider the bridging faults in the five-transistor group of the FSB (GSB) according to Fig. 13a. There is only one bridging fault, which is between node S_j (see Fig. 13a) and node N_F (N_G), that is not detectable for any value of the corresponding bridging resistance R_{BR10}. Consequently, from the layout design point of view, our decision was to turn away these two nodes so that it is impossible for this fault to appear (in our layout, their distance is seven times the minimum wire distance of the corresponding metal layer in the used technology). The values of the maximum bridging resistances that are detectable in the five-transistor group are shown in Table 5.

Possible bridging faults in the current mirror and the output inverter are illustrated in Fig. 13b, while, in Table 5, the maximum detectable resistance values are presented.

Possible bridging faults in the NOR gate and the DFF of CSR are presented in Figs. 13c and 13d, respectively. The maximum detectable resistance values for both circuits are also provided in Table 5.

6.7 Suitability to Implement Embedded Checkers

With regard to the SA, TSOP, TSON, transient, and bridging faults, the proposed checker needs the application of only

Fig. 13. Possible bridging faults (a) in the five-transistor group of FSB (GSB), (b) in the current mirror and output inverter, (c) in the NOR gate, and (d) in the DFF of CSR.

TABLE 5
Maximum Detectable Bridging Resistance Values

The five transistor group

R_{BR1}	R_{BR2}	R_{BR3}	R_{BR4}	R_{BR5}	R_{BR6}	R_{BR7}	R_{BR8}	R_{BR9}	R_{BR10}	R_{BR11}	R_{BR12}	R_{BR13}	R_{BR14}	R_{BR15}
800Ω	100KΩ.	25KΩ	16KΩ	1.4KΩ	4.5KΩ	9KΩ	16KΩ	16KΩ	16KΩ	16KΩ	16KΩ	16KΩ	8KΩ	8KΩ

The current mirror

R_{BR1}	R_{BR2}	R_{BR3}	R_{BR4}	R_{BR5}	R_{BR6}	R_{BR7}	R_{BR8}
50KΩ	25KΩ	10KΩ	20KΩ	7KΩ	8kΩ	4KΩ	12KΩ

The NOR gate

R_{BR1}	R_{BR2}	R_{BR3}	R_{BR4}	R_{BR5}	R_{BR6}	R_{BR7}	R_{BR8}	R_{BR9}
12KΩ	100KΩ	10KΩ	8KΩ	>100KΩ	5KΩ	8KΩ	40KΩ	5KΩ

The D Flip-Flop of CSR

R_{BR1}	R_{BR2}	R_{BR3}	R_{BR4}	R_{BR5}	R_{BR6}	R_{BR7}	R_{BR8}	R_{BR9}	R_{BR10}	R_{BR11}	R_{BR12}
100KΩ	100KΩ	4KΩ	100KΩ	100KΩ	20KΩ	100KΩ	100KΩ	0.5KΩ	100KΩ	100KΩ	6KΩ

two codewords (out of the 2^{n-1} equivalent codeword pairs) to satisfy the TSC or SCD properties, similarly to the checkers presented in [13], [16], [17], [18]. The only requirement for these two codewords is to have complementary bit pairs $(X_j, Y_j\ j \in [1, \dots, n])$ between each other, for instance,

$$(X_1Y_1, \dots, X_jY_j, \dots, X_nY_n)_A = (10, \dots, 10, \dots, 10)$$

and

$$(X_1Y_1, \dots, X_jY_j, \dots, X_nY_n)_B = (01, \dots, 01, \dots, 01).$$

Consequently, as was proven in [18], the parallel TRC checkers, like the proposed one, require, on average, less than half the codewords required by the corresponding tree-structured TRC checkers (composed of two-input TRC checkers) to satisfy the ST property. This is a very important property for an embedded checker, as we discussed in Section 1, which makes the proposed design approach a suitable solution (over tree-structured TRC checkers) for embedded TRC checkers.

7 Conclusions

In this paper, we have presented a current mode parallel TRC checker suitable for the implementation of high fan-in embedded checkers. The new circuit belongs to the periodic output category of TRC checkers and provides high testability since it is TSC or SCD for a wide set of realistic faults, including TSOP faults that are not covered by other TRC checkers in the same class. Designs of this TRC checker, for various numbers of inputs (n-values), in a standard 0.18μm CMOS technology and the subsequent extended simulations (in a full range of process, voltage, and temperature conditions) proved the efficiency of the circuit over earlier topologies in the same category in terms of silicon area requirements, speed performance, and power consumption (especially for high n-values).

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