A High Speed Circuit for Concurrent Detection of Soft Errors in CMOS ICs

S. Matakias, Y. Tsiatouhas, A. Arapoyanni and Th. Haniotakis

***Abstract*— A new circuit that exploits the temporal nature of transient faults to provide concurrent soft error detection is presented in this work. The idea is based on a current mode sense amplifier topology to achieve small error detection times and on a high density pre-sensing scheme to reduce silicon area requirements.**

***Index Terms*—Concurrent Transient Fault Detection, Error Detection, Soft Error Detection, Sense Amplifier.**

I. INTRODUCTION

The device size scaling, the increased operating frequency and the power supply reduction that follow process evolution affect modern ICs reliability. Thus, single event upsets (SEUs) and single event transients (SETs), due to alpha particles and cosmic-ray secondary neutrons [1-4], play an important role to transient fault and consequently soft error generation in nanometer CMOS technologies.

The generated transient pulses (faults) on internal circuit nodes of a CMOS IC can propagate towards the combinational logic outputs. These pulses are often attenuated before they reach an output. Furthermore, even if they reach an output they will contribute to a soft error generation only if they occur during the time at which the clock samples this output. However, since the clock frequency increases, the probability that the transient pulse is captured by the clock edge also increases. Thus, transient faults lead to increased and many times unacceptable soft error rate (SER) levels in today and future technologies and consequently logic parts will require protection against soft errors analogous to this developed earlier for memories [5-6]. Obviously, on-line testing techniques are becoming mandatory in order to achieve acceptable levels of soft error robustness.

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Duplication and triplication techniques are widely used to achieve systems reliability. However, the extra cost, in power consumption and silicon area makes them impractical for a wide variety of electronic circuits. As an alternative approach, concurrent checking schemes combined with a retry procedure after an error detection, can be considered. Self-checking design is a possible candidate but it may also require high hardware cost [11]. Recently, soft error detection techniques have been proposed in the open literature [7-13] that are based on the temporal nature of the transient faults to provide error tolerance using time redundancy.

In this work we present a new soft error detection circuit that also exploits the temporal nature of transient faults. The circuit is characterized by high operating speed (small detection times) and low silicon area requirements. The paper is organized as follows. In section 2 the new concurrent soft error detection scheme is introduced and discussed. In section 3 simulation results are provided in order to validate this approach and explore its feasibility in future technologies. Finally, the conclusions are drawn in section 4.

II. THE PROPOSED ERROR DETECTION CIRCUIT

Fig. 1 presents a Functional Circuit consisting of the combinational part and the flip-flops of the output register. Transient faults on internal nodes of the combinational logic may result in the appearance of transient pulses at its output lines *OUT*. In case that the triggering edge of the clock *CLK* arrives just after the transient pulse appearance and during its presence on the *OUT* line (time interval δ), a soft error is generated at the output *FFO* of the flip-flop.

The key idea behind the adopted error detection technique is the use of a Monitoring Circuit to compare the responses at the outputs of the combinational part (*OUT*) and the primary outputs (*FFO*) of the Functional Circuit (see Fig. 2) after a time interval δ_{max} from the latching edge of the clock signal *CLK* [7-13]. The time interval δ_{max} is equal to the maximum transient pulse duration that must be detectable in order to achieve an acceptable soft error rate level.

In the fault free case no signal transitions appear on the monitored lines after the latching edge of the clock signal *CLK*. Thus, *OUT* and *FFO* present equal values and the error indication signal of the Monitoring Circuit remains "low" (*ERR*="low"). The presence of a transient fault in the combinational logic may cause a transient pulse on one of its output lines *OUT* when the latter is sampled by the clock *CLK*. In that case, the Output Flip-Flop captures an erroneous value (see Fig. 1(b)) and a soft error occurs on its output *FFO*.

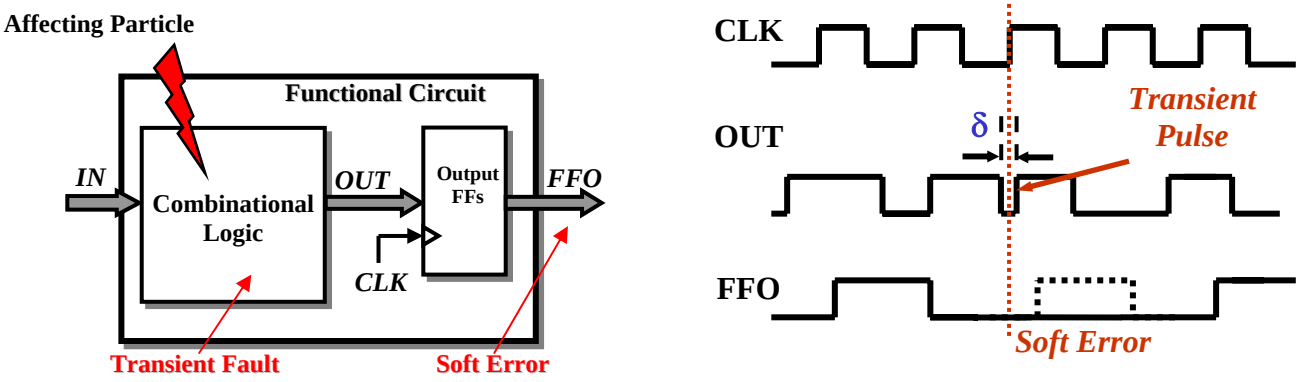

Figure 1: Soft error generation mechanism

Then, after the expiration of the transient pulse duration time (δ), the output line *OUT* turns to its correct value. The Comparator (Comp) detects the resulted difference between the values on the lines *OUT* and *FFO* and raises its output to "high". This value is latched in the Error Indication Flip-Flop (EIFF) by the *SCLK* signal and *ERR* rises to "high" (*ERR*="high") indicating the error presence. The *SCLK* signal is a delayed version of *CLK* by a time interval equal to $\delta_{max}+D_{SA}$, where D_{SA} the delay of the Sense Amplifier.

In this paper we propose a new Monitoring Circuit for soft error detection that is originated from sense amplifier based signal amplification techniques. Sense amplifiers are widely used in semiconductor memories to retrieve the stored data in a memory array by amplifying small signal variations on their inputs. The proposed Monitoring Circuit is shown in Fig. 3 and consists of a Sense Amplifier (SA), a Pre-Sensing Block (PSB) and an Error Indication Flip-Flop (EIFF). The Pre-Sensing Block is divided into two sub-blocks (SBL and SBR) each one feeding a separate input of the sense amplifier *INL* and *INR* respectively. The k pairs of monitored lines OUT_j and FFO_j (j∈[1 .. k]), are driving both the sub-blocks of the Pre-Sensing Block.

Each sub-block consists of 2k nMOS transistors. In the left sub-block the 2k pairs of transistors are connected in parallel between the V_{DD} power supply (through an nMOS transistor - MFL) and the left input *INL* of the sense amplifier. In addition a single nMOS transistor (MCL) is connected between the Gnd power supply and *INL*, which is driven by the enable signal *EN*. Each path formation between the power supply V_{DD} and *INL* through MFL and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCL. In the right sub-block a quite similar topology is present. An identical arrangement of 2k pairs of transistors is connected between the Gnd power supply (through an nMOS transistor - MFR) and the right input *INR* of the sense amplifier. A single nMOS transistor (MCR) is connected between the V_{DD} power supply and *INR*, which is also driven by the enable signal *EN*. Each pair is driven in exactly the same way as in the case of the left sub-block and each path formation between the power supply Gnd and *INR* through MFR and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCR.

The Sense Amplifier is activated by the *EN* signal and provides the output signal *SAO*, which is latched by the Error Indication Flip-Flop (EIFF) at the rising edge of signal *SCLK*.

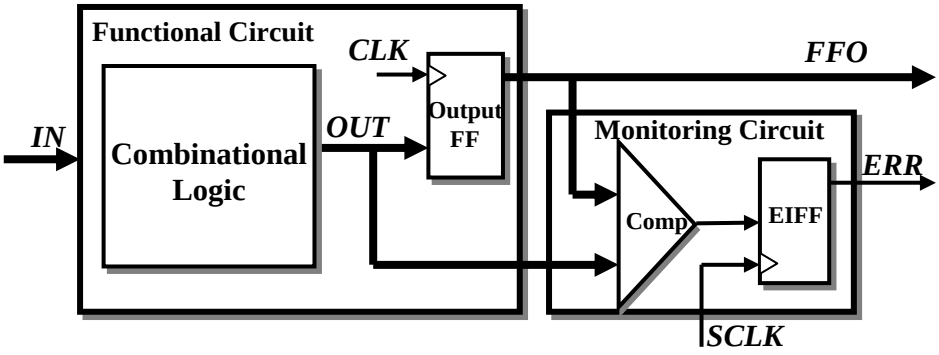

Figure 2: The soft error detection topology

In the error free case where OUT_j=FFO_j (∀ j∈[1...k]) during the monitoring phase, there is no path formation between the inputs *INL* and *INR* of the Sense Amplifier and the power supplies V_{DD} and Gnd respectively, through the Pre-Sensing Block. Thus, the input *INL* of the Sense Amplifier is discharged through the transistor MCL while the input *INR* is charged through the transistor MCR. The Sense Amplifier will amplify the signal difference between its two inputs driving fast its output *SAO* to "low".

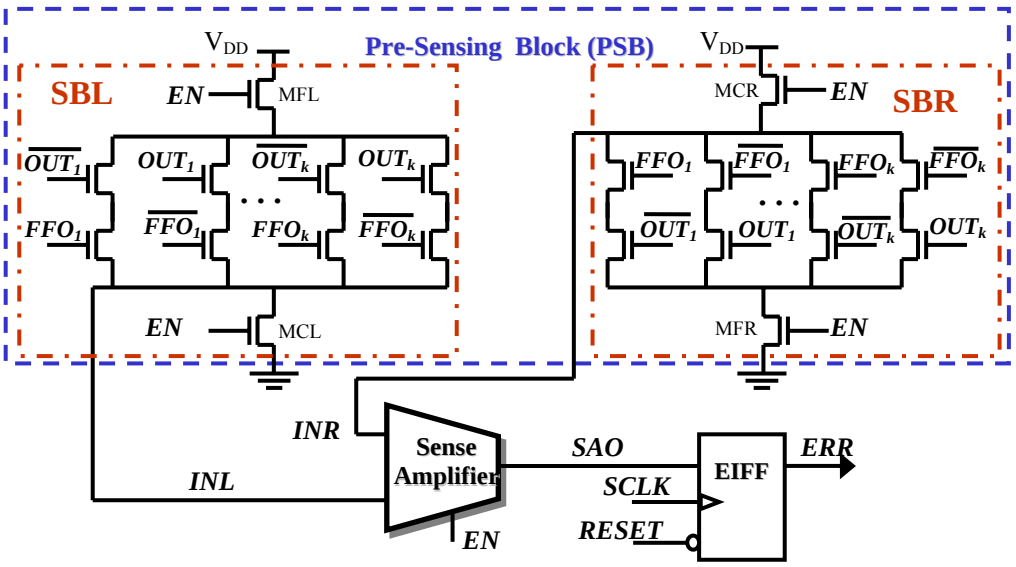

Figure 3: The proposed Monitoring Circuit

In the presence of an error there will be at least a pair of monitored lines such that $OUT_j \neq FFO_j$ ($j \in [1 \ldots k]$). Thus, there will be at least one path formation between *INL* and V_{DD} as well as a path formation between *INR* and Gnd. Since the established paths are dominant compared to the paths through transistors MCL and MCR respectively, the input *INL* of the Sense Amplifier is charged while the input *INR* is discharged. Also in that case, the Sense Amplifier will amplify the signal difference between its inputs driving fast its output *SAO* to "high".

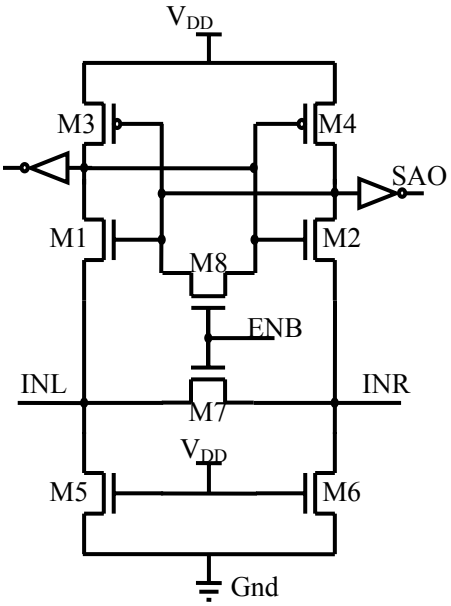

Figure 4: Sense Amplifier Circuit

This response is latched by the Error Indication Flip-Flop at the rising edge of *SCLK* turning signal *ERR* to "high" and providing the indication of an error detection. The *ERR* line remains "high" until the *PRESET* signal is activated after the proper actions of the system to handle the erroneous situation.

III. CIRCUITS AND SIMULATION RESULTS

In the design of the Monitoring Circuit presented in the previous section, the current mode, self-precharged Sense Amplifier proposed in [14] has been used (see Fig. 4), which provides extremely small sensing delay times since its response times are almost independent of the capacitance load on its inputs [15]. The Sense Amplifier operates in two phases, the precharge/equalization and the sensing. A precharge/equalization phase always precedes a sensing phase and is used to set the internal nodes of the Sense Amplifier to proper voltage levels as well as to equalize the voltage level on its inputs. The Sense Amplifier under consideration is a self-precharged circuit. During the time period where *EN*="low" the Sense Amplifier is in the precharge/equalization phase. The sensing phase is activated when *EN* turns to "high" and is identical to the monitoring phase of the Monitoring Circuit.

Since the Pre-Sensing Block has been designed with the use of only nMOS transistors, the Monitoring Circuit presents a very stable behaviour under process variations. Layout design techniques like these commonly used in memory array design (folded bit-lines etc) can be exploited in order to achieve a high density Pre-Sensing Block and improve further the behaviour of the Monitoring Circuit making it tolerant in process and temperature variations.

The proposed circuit has been designed in the 0.18μm CMOS technology of ST Microelectronics (V_{DD}=1.8V) The simulated waveforms of the signals *EN*, *OUT* and *FFO* as well as the response signal *SAO* of the Sense Amplifier are presented in Fig. 5, for the case of 72 monitored pairs and for typical transistor models in 27° C. The upper curves of Fig. 5 show the signals *OUT* and *FFO* of the Functional Circuit under monitoring, while in the middle curve the waveform of the *EN* signal is drawn. Finally, the lower curve shows the response (pass/fail) signal *SAO* of the Sense Amplifier. Five cases are presented. In the first two and the fourth both signals *OUT* and *FFO* have equal values (either high or low), during

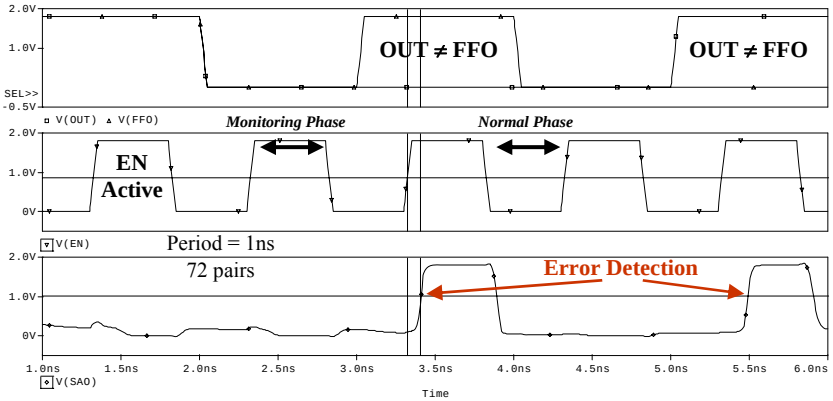

Figure 5: Simulated waveforms

the time interval of the monitoring phase, while in the third and fifth the two signals are complementary (*OUT*="low", *FFO*="high" and *OUT*="high", *FFO*="low" respectively). Only in the latter cases the output of the Sense Amplifier turns "high", just after the enable signal *EN* goes active ("high"), indicating the detection of the error.

TABLE I

Number of Monitored Pairs	Detection Time (ps)		Reduction %
	[13]	Proposed	
9	456	191	58
18	501	226	55
36	581	265	54
72	721	317	56
144	979	376	62
288	1485	430	71
576	2480	468	81

Similar simulations have been carried out for various numbers of monitored pairs (from 9 to 576), for temperatures up to 125°C and using all technology corners for the transistors' parameters in the design. Comparisons with a high speed error detection circuit, presented in [13], are shown in Table I to validate the performance of the proposed scheme.

IV. CONCLUSIONS

In this paper we presented a monitoring circuit for concurrent detection of soft errors in CMOS ICs which is based on the use of a fast sense amplifier topology. The circuit exploits the temporary nature of the transient faults to detect the corresponding errors that appear at the outputs of the circuit being monitored. According to the experimental results, large detection time reductions, higher than 50%, can be achieved that are increased with the number of lines under monitoring.

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