Fast, Parallel Two-Rail Code Checker with Enhanced Testability*

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Abstract

A current mode, periodic outputs, parallel two-rail code (TRC) checker, suitable for high n-variable (high fan-in) implementations, is presented. The new checker is characterised by high testability, high operating frequencies and low silicon area requirements. The circuit has been designed, for various n-variable values, in a 0.18μm technology and SPICE simulations have been carried out to validate its operation.

1. Introduction

Modern semiconductor technology applications are characterized by an increased demand for high reliability. Self-Checking Circuits (SCC) [1] are a widely used solution due to their ability to detect errors on-line during the normal operation. A SCC consists of a functional circuit (the Circuit Under Monitoring) whose outputs are monitored by a checker. The Circuit Under Monitoring is designed to provide output codewords, that belong to an error detecting code, in the fault free case and non codewords in the presence of a fault. The checker produces an error indication signal whenever the Circuit Under Monitoring produces a non codeword output. In addition, in case of checker's internal faults, it must also provide an error indication. The above requirements are covered by the Totally Self-Checking (TSC) [2] and the Strongly Code-Disjoint (SCD) [3] properties.

The special category of the two-rail code (TRC) checkers [1] is exploited to check the correctness of input words with n pairs of two-railed bits [4-8]. In that case they are called n-variable TRC (TRC_n) checkers. Usually n-variable TRC checkers, with n>2, are implemented as a tree of 2-variable TRC checkers. Obviously, for large n the performance and the required silicon area of tree TRC checkers make them a non attractive solution for today applications. Non-tree TRC checkers with periodic outputs have been proposed in [9-12]. The main drawback of these checkers is that, in high n-variable implementations, they present a considerable degradation of their speed performance and increased requirements in silicon area while in many cases stuck-open faults are not covered. Recently, in [13] a very fast and low cost parallel TRC checker (or equality checker) is proposed targeting high fan-in applications, but also in that case the non testability of a number of stuck-open faults still remains a drawback.

In this paper we modify and extend the checker in [13] to be able to cover the non-testable stuck-open faults. According to the ITRS Roadmap [14] these faults are of great interest in very deep submicron technologies. The checker is based on current mode design techniques to implement an equivalent XNOR-OR tree of n-pairs of inputs. This structure provides concurrent error detection with very short response times and low silicon area requirements. Moreover, this TRC checker is proved to be TSC or SCD for a wide set of realistic faults including also those transistor stuck-open faults not covered in [11-13]. In addition, like in [9-13], the checker requires only two input code words (out of a wide variety of equivalent pairs) to satisfy the TSC and SCD property for the enhanced set of faults.

The manuscript is organized as follows. In Section 2 the topology and the operation of the proposed TRC checker are analyzed and its code-disjoint property is proved. Next, in Section 3 the self-checking property of the circuit, with respect to stuck-at, stuck-open, stuck-on and transient faults, is discussed. Design issues are covered in Section 4 and simulation results are presented in a 0.18μm CMOS technology along with comparisons with the checker in [11]. Finally, Section 5 provides the conclusions.

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2. The proposed two-rail code checker

The general topology of a circuit that is monitored by a two-rail code (TRC) checker is shown in Fig. 1. The Circuit Under Monitoring is designed to produce two-railed output words (X_j, Y_j, j=1,2,…,n) when it is fault-free ($X_j=\overline{Y_j}$) and non two-railed output words ($X_j=Y_j$) in case of internal faults. The TRC checker verifies whether the output words of a Circuit Under Monitoring are two-railed or not, providing the two-railed output indication signals F and G.

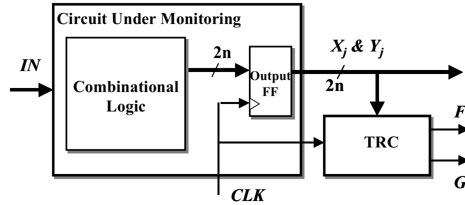

Fig. 1. A SCC with a TRC checker

The proposed *n*-variable pairs (X_j, Y_j, j=1,2,…,n) TRC checker is presented in Fig. 2. It is divided into two sub-blocks, the F-SubBlock (FSB) and the G-SubBlock (GSB). The first sub-block is fed by half of the inputs (X_r, Y_r, r=1,2,…,k, where k=n/2) and the second by the rest of the checker inputs (X_s, Y_s, s=k+1,k+2,…,n). Each pair of inputs (X_j, Y_j) drives a pair of serially connected pMOS transistors and a pair of serially connected nMOS transistors in the corresponding sub-block.

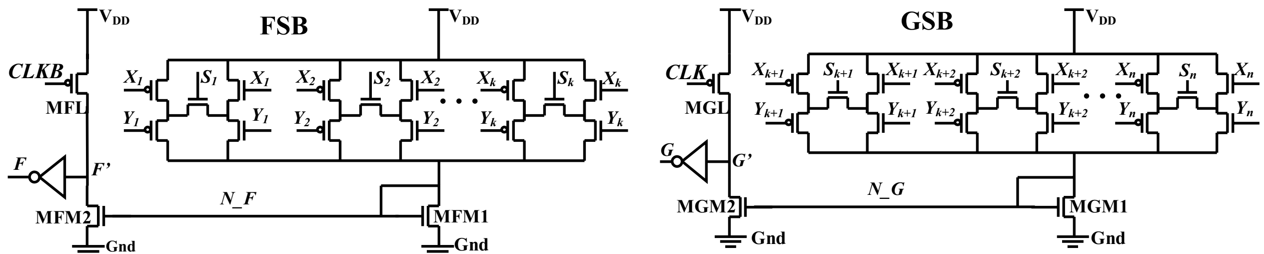

Figure 2. The proposed two-rail code checker

Thus, there are n-pairs of transistors in each block connected in parallel between the V_{DD} power supply and the input terminal of a current mirror. In each group of two pairs of transistors, a pMOS and an nMOS pair, driven by the same combination of inputs (X_j, Y_j), there is a fifth nMOS transistor that is controlled by a select signal S_j and "connects" the two pairs. This transistor is used to enhance the testability of the group. The current mirrors are formed by two nMOS transistors in each sub-block, transistors MFM1 - MFM2 and MGM1 - MGM2 respectively. Finally, the pMOS transistors MFL and MGL are used as loads at the output terminals of the FSB and GSB respectively. The MFL transistor is driven by the *CLKB* signal and the MGL by the *CLK* signal.

The select signals S_j (j=1,2,…,n) are generated by a Cyclic Shift Register (CSR) of k=n/2 bits and a NOR gate array, as it is shown in Fig. 3. The CSR is loaded with a pattern which has only one bit position with the "0" value. When *CLK*="1", then S_r="0" (∀ r=1,2,…,k) while only one S_s signal (s=k+1,k+2,…,n) has the value "1", this related to the bit position in the CSR with the "0" value. In symmetry, when *CLK*="0" then S_s="0" (∀ s=k+1,k+2,…,n) while only one S_r signal (r=1,2,…,k) has the value "1", also this related to the bit position in the CSR with the "0" value.

The checker's output nodes F and G always present complementary logic values in the fault free case and non-complementary in the opposite case providing the indication of the correct system operation or not. The checker operation is divided into two phases, transparent to the Circuit Under Monitoring, according to the clock *CLK* semi-periods. In the fault free case ($X_j=\overline{Y_j}$ ∀ j=1,2,…,n) and for each phase the following stand:

a) In the first semi-period, when *CLK*="1", each pair of transistors driven by the inputs (X_r, Y_r, r=1,2,…,k), in the FSB, has one transistor in the non conducting state while all the transistors driven by the signals S_r are in the non conducting state. Thus, no current passes through the pertinent current mirror forcing F' to be charged to V_{DD} through MFL which is in the conducting state. However, there is a single transistor in the GSB, driven by an S_s signal (s=k+1,k+2,…,n), that is in the conducting state. Thus, there will be a current path from V_{DD} to the input terminal (*N_G*) of the corresponding current mirror through this transistor and the two conducting transistors, a pMOS and an nMOS transistor, of the pertinent pairs depending on the input combination (X_s, Y_s). No other current path is formed. Since the MGL transistor is in the non-conducting state the mirrored current that is generated discharges node G' towards

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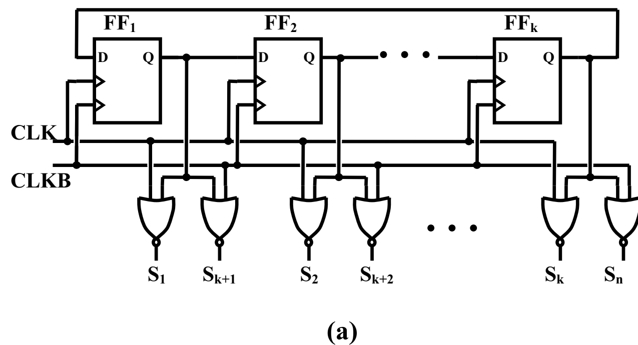
Gnd. Consequently F and G present complementary values ("0" and "1" respectively) in the first semi-period of the clock.

b) Similarly, in the second semi-period when CLK="0", the opposite case stands setting also F and G to complementary values, "1" and "0" respectively.

Thus, in the fault free case, nodes F and G are always in complementary states (two-railed) at the end of each clock semi-period.

In case that a non two-rail word is present at the inputs of the checker, at least one input pair (X_j, Y_j) has equal values (X_j=Y_j). Three cases are observed: i) all the non two-rail input pairs feed the FSB, ii) all the non two-rail input pairs feed the GSB and iii) there are some non two-rail pairs that feed the FSB and the rest the GSB.



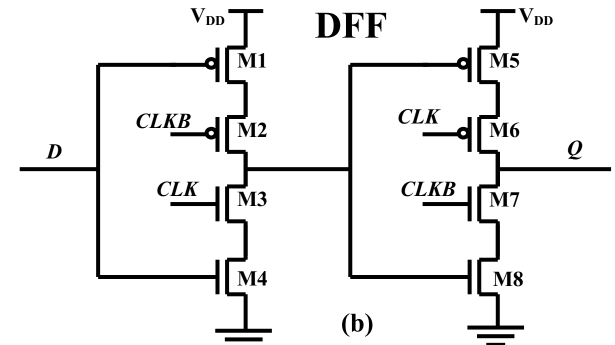


Figure 3. (a) Select signal generation circuitry, (b) The D Flip-Flop

In case (i) there is at least one pair of serially connected transistors in FSB, driven by the non two-rail input pair that will be in the conducting state (either a pMOS pair when X_j = Y_j = "0" or an nMOS pair when X_j = Y_j = "1"). Thus, in the first semi-period of the clock there will be a current flow through the current mirror of the FSB which will discharge (or keep discharged) node F', since the current mirror is designed to be more conductive (dominant) over the load transistor MFL. Consequently, the F node turns to "1" and since the GSB operation does not depend on the input values during the first semi-period, both F and G will be in the "1" state indicating the presence of the error.

Similarly, in the second case (ii) the current mirror of the GSB is more conductive over the load transistor MGL and in the presence of the error will discharge (or keep discharged) node G'. Consequently, the G node turns to "1" and since the FSB operation does not depend on the input values during the second semi-period, both F and G will be in the "1" state indicating the presence of the error.

Finally, in case (iii) an erroneous pair of inputs affects both FSB and GSB. Consequently, according to (i) and (ii), F and G will be in the "1" state in both semi-periods of the clock indicating the presence of the errors.

From the above analysis it is obvious that the circuit is fault secure since, for every fault, never produces an incorrect output codeword for all input codewords.

3. The self-checking property of the checker

In this section the self-checking property of the proposed checker is discussed with respect to a set of faults consisting of: 1) line stuck-at faults, 2) transistor stuck-on faults, 3) transistor stuck-open faults and 4) transient faults. The following two common assumptions in the checker design [2] have been taken into account: i) a single fault occurs at a time and ii) the time between two successive faults is enough to permit the application of all possible (required) codewords.

3.1 Line stuck-at faults

We can observe five cases of possible line stuck-at (SA) faults in the circuit shown in Fig. 2: a) SA faults on the input lines of the checker X_j, Y_j, j=1,2,…,n , b) SA faults on the select lines S_j, c) SA faults on the checker outputs F and G, d) SA faults on the internal lines of the checker N_F, F', N_G and G' and e) *CLK* or *CLKB* signal lines SA faults.

a) SA faults on the input lines X_j, Y_j, j=1,2,…,n of the checker are equivalent to non two-rail words on them. Therefore, the checker is TSC with respect to these faults.

b) A SA "0" on a select signal S_j will result in no current path formation in the corresponding sub-block FSB (GSB) during the second (first) semi-period when S_j should be "1". Thus, both F and G will be "0" during this semi-period. A SA "1" on a select signal S_j will

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result in a current path formation during the first (second) semi-period where no conducting path should exist in the FSB (GSB). Consequently, both F and G will be "1" during this semi-period. Therefore, the checker is TSC with respect to these faults.

c) Obviously, the checker is TSC considering SA faults on the output lines F or G.

d) A SA "0" or "1" fault on N_F (N_G) is equivalent to a SA "0" or "1" fault on the F (G) output of the checker. Similarly, a SA "0" or "1" fault on F' (G') will result in a SA "1" or "0" response on the output F (G). Consequently, according to (c), the checker is TSC for this kind of faults.

e) A SA "1" fault on the *CLK* (*CLKB*) lines that drive the load transistors in GSB (FSB) will result in a SA "1" value on line G (F) and the circuit is TSC with respect to this fault. However, a SA "0" fault on these lines cannot be detected but also does not affect the circuit logic operation although it increases the power consumption. The checker is proved to be SCD for this fault.

3.2 Transistor stuck-open faults

Transistor stuck-open (TSOP) faults can be categorised into four groups: a) on the transistors that are driven by the checker inputs (X_j, Y_j, j=1,2,…,n), b) on the transistors that are driven by the select signals S_j, c) on the transistors that are driven by the clock signals *CLK* and *CLKB* and d) on the transistors of the current mirrors.

a) A TSOP fault on a transistor of the FSB (GSB) that is driven by a checker input X_j or Y_j, is detectable since there exists an input codeword with (X_j, Y_j) = (0, 1) or (1, 0) respectively to sensitise it. In the presence of the fault and after the application of this codeword at the checker inputs, no current path can be formed in the FSB (GSB) during the second (first) semi-period and during the timeframe when S_j is "1" although the transistor under test should be in a conducting state according to its gate value. In that case, both F and G will be "0" during this semi-period and consequently, the checker is TSC with respect to these faults.

b) A TSOP fault on a transistor that is driven by a select signal S_j will result in no current path formation in the corresponding sub-block FSB (GSB) during the second (first) semi-period when S_j is "1". Thus, both F and G will be "0" during this semi-period and the checker is TSC with respect to these faults.

c) When the transistor MFL (MGL) is affected by a TSOP fault, the output F (G) of the checker is "1" during the first (second) semi-period and thus the fault is detectable. Consequently, the checker is TSC with respect to these two faults.

d) Finally, a TSOP fault in the MFM1 (MGM1) transistor will lead node N_F (N_G) to be permanently charged to V_{DD}. Thus, transistor MFM2 (MGM2) will be always in the conducting state turning F (G) to "high" during the first (second) semi-period of the clock. Consequently, the checker is TSC for this fault. Moreover, a TSOP fault on MFM2 (MGM2) will result in a "low" value at the F (G) output of the checker during the second (first) semi-period of the clock. Hence, the checker is also TSC for this fault.

3.3 Transistor stuck-on faults

Similarly to the TSOP faults, transistor stuck-on (TSON) faults can be categorised into four groups: a) on the transistors that are driven by the checker inputs (X_j, Y_j, j=1,2,…,n), b) on the transistors that are driven by the select signals S_j, c) on the transistors that are driven by the clock signals *CLK* and *CLKB* and d) on the transistors of the current mirrors.

a) A TSON fault on a transistor of the FSB (GSB) that is driven by the checker inputs X_j or Y_j, j=1,2,…,n is detectable since there exists an input codeword that tries to set this transistor in the non-conducting state. After the application of this codeword at the checker inputs there will be a current flow through the current mirror of the FSB (GSB), due to the presence of the fault, which will set node F' (G') to "low" during the first (second) semi-period of the clock, since the current mirror is designed to be more conductive (dominant) over the load transistor MFL (MGL). Thus node F (G) will be to the "high" state during this semi-period and the fault will be detected. Consequently, the checker is TSC for this kind of faults.

b) A TSON fault on a transistor that is driven by a select signal S_j will result in a current path formation in the corresponding sub-block FSB (GSB) during the first (second) semi-period. As in case (a) node F (G) will be "1" during this semi-period and thus, the checker is TSC for this kind of faults.

c) A TSON fault on the MFL (MGL) transistor does not affect the checker's logical behaviour but increases the power consumption. Concerning this fault, it is proved that the checker is SCD.

d) The presence of a TSON fault on transistor MFM1 (MGM1) will prohibit any current flow through the left branch of the current mirror, that is transistor MFM2 (MGM2), resulting in a "low" value on the F (G) output of the checker during the second (first) semi-period of the clock. Thus, this kind of fault is detectable and the checker is TSC with respect to this fault. Moreover, a TSON fault on transistor MFM2 (MGM2) will lead to a "high" value at the output F (G) of the checker during the first (second) semi-period of

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the clock. Therefore, the checker is TSC for a TSON fault on transistor MFM2 (MGM2).

3.4 Transient faults

Considering possible transient faults, for instance a transient pulse due to a single event upset in a checker's node, two cases exist. Either the transient pulse is attenuated in the internal nodes of the checker without affecting the outputs F and G and the checker satisfies the SCD property, or the effect of the pulse is propagated to an output (F or G) where it will be detected and the checker is TSC for this type of fault.

3.5 The select signal generation circuitry

The circuit that generates the select signals S_j it is presented in Fig. 3(a). The D Flip-Flop (DFF) used in the CSR is shown in Fig. 3(b) and has been selected due to its high testability and its low silicon area requirements. Aiming that the circuit meets the self-checking property, we have inserted a pair of serially connected pMOS transistors in both the FSB and the GSB sub-blocks that are driven directly by two successive stage outputs of the CSR (e.g. FF1 and FF2), as it is shown in Fig. 4.

i) Stuck-at faults:

a) A SA "1"at an output of a Flip-Flop of the CSR (or equivalently the pertinent input of a NOR gate) will result in an all "1" state of the CSR after at most k clock cycles. In that case, no select signal S_j can be activated, resulting to "0" responses in both F and G.

b) Similarly, a SA "0" at an output of a Flip-Flop of the CSR (or equivalently the pertinent input of a NOR gate) will result in an all "0" state of the CSR after at most k clock cycles. In that case both the two pairs of pMOS transistors driven by FF1 and FF2 in the FSB and GSB sub-blocks will be in a conducting state for a whole clock period. Thus, both F and G will be "1".

c) A SA "0" or "1" fault at the CLK input of a DFF is equivalent to a SA "1" fault at the output of this DFF, while a SA "0" or "1" fault at the CLKB input of a DFF is equivalent to a SA "0" fault at the output of this DFF. Thus, these faults are covered by (a) and (b).

d) A SA "1" at the clock input of a NOR gate will result in a SA "0" value on its output so that the corresponding select signal S_j could not be activated. Consequently, there will not be any current path formation during the second (first) semi-period in the pertinent sub-block FSB (GSB), so that both F and G will carry a "0" value.

e) A SA "0" at the clock input of a NOR gate will result in the activation of the corresponding select signal S_j for a whole clock period. Consequently, there will be a current path formation during the first (second) semi-period in the pertinent sub-block FSB (GSB), so that both F and G will carry a "1" value.

f) A SA "1" at the output of a NOR gate is equivalent to the previous case (i.e).

g) Finally, a SA "0" at the output of a NOR gate is equivalent to the case (i.d).

Thus, the circuit is TSC with respect to the faults of the classes (i.a) - (i.g).

ii) Transistor stuck-open faults:

a) A TSOP fault on transistor M1 or M2 or M7 or M8 in a DFF of the CSR will result in a permanent "1" value on its output. Consequently, the CSR turns to the all "1" state after at most k clock cycles and this case is equivalent to that in (i.a).

b) A TSOP fault on M3 or M4 or M5 or M6 in a DFF of the CSR will result in a permanent "0" value on its output. Consequently, the CSR turns to the all "0" state after at most k clock cycles and this case is equivalent to that in (i.b).

c) A TSOP fault on a pMOS transistor of a NOR gate will result in a permanent "0" value at the gate output after its first discharge. This case is equivalent to the case (i.c).

d) A TSOP fault on the nMOS transistor of a NOR gate that is driven by the clock signal will result in a permanent "1" value at the gate output during a whole clock period when the output of the corresponding DFF is "0". This case is equivalent to the case (i.d).

e) A TSOP fault on the nMOS transistor of a NOR gate that is driven by the output of the corresponding DFF will never affect the circuit operation since this transistor is redundant. This is due to the fact that the "00" input state of the NOR gate is always followed by the state where at least the clocked input turns to "1". Thus the gate output is discharged and remains discharged in the subsequent semi-period when the clocked input turns to "0" although the DFF output is "1" (memory state). A subsequent TSOP fault on the transistor that is driven by the clocked input will result in a permanent "1" value at the output of the NOR gate and this case is equivalent to the case (i.d).

Thus, the circuit is TSC with respect to the faults of the classes (ii.a) - (ii.d) and SCD for the class (ii.e).

f) A TSOP fault on a transistor of the FSB or GSB that is driven either by the FF1 or FF2 signal is not detectable. One way is to test these transistors off-line just after the system power-up. In that case a pattern with two successive "0" states is inserted in the CSR. When FF1 and FF2 are both "0", then in the fault free case the outputs F and G are both "1", in other case a TSOP fault is detected. However, note that one of the

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two pairs is redundant which reduces the probability such a fault to alter the circuit operation. This off-line testing operation can also cover global clock (CLK or CLKB) SA faults.

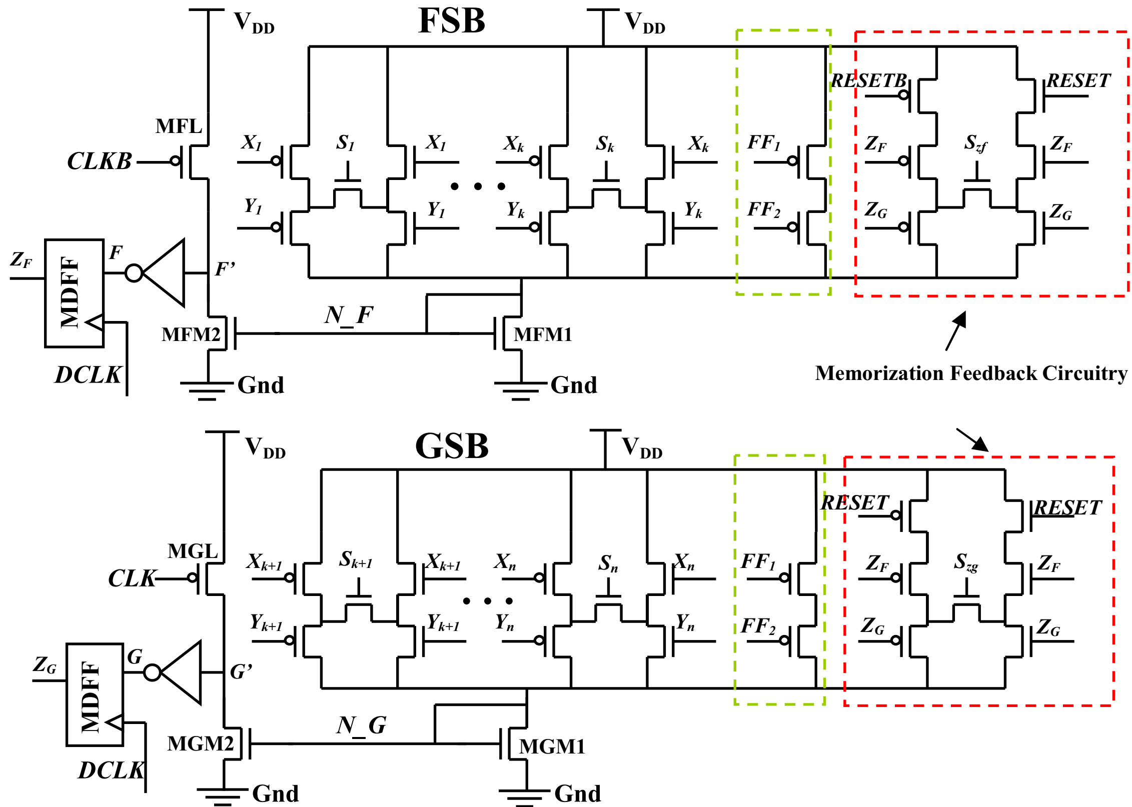

Figure 4. The complete checker design

iii) Transistor stuck-on faults:

a) A TSON fault on transistor M1 or M8 in a DFF of the CSR will result either in successive "0" responses of the cell or it will not have an effect on the circuit operation, depending on the transistor strength. In the first case, as in (i.b), after at most k clock cycles both the two pairs of pMOS transistors driven by $FF1$ and $FF2$ in the FSB and GSB sub-blocks will be in a conducting state for a whole clock period. Thus, both F and G will be "1" and the circuit is TSC. In the second case it is proved that the circuit is SCD.

b) A TSON fault on transistor M2 or M7 in a DFF of the CSR will result in a sequence of "0" responses of the cell and according to the previous case (iii.a) the circuit is TSC.

c) A TSON fault on transistor M4 or M5 in a DFF of the CSR will result either in the deletion of the "0" state from the register or it will not have any effect on the circuit operation, depending on the transistor strength. In the first case, as in (i.a), no select signal S_j can be activated, resulting to "0" responses in both F and G and the circuit is TSC. In the second case it is proved that the circuit is SCD.

d) A TSON fault on transistor M3 or M6 in a DFF of the CSR will result in the deletion of the "0" state from the register and according to the previous case (iii.c) the circuit is TSC.

e) In the case of the NOR gates the decision is to make the nMOS transistors dominant (more conductive) over the pMOS transistors. This way a TSON fault on a pMOS transistor does not affect the circuit operation and the circuit is SCD with respect to this fault. However, a TSON fault on an nMOS transistor will result in a permanent "0" response of the gate and thus according to (i.f) the circuit is TSC.

Note that with regard to the SA, TSOP and TSON faults, the proposed checker needs the application of only two codewords (out of the 2^n possible codewords) to satisfy the TSC or SCD properties, similarly to the checkers presented in [9-13]. The only requirement for these two codewords is to have complementary pairs (X_j, Y_j, j=1,2,…,n) between each other, for instance $(X_1Y_1,\ldots,X_jY_j,\ldots,X_nY_n)_A$=(10,…,10,…,10) and $(X_1Y_1,\ldots,X_jY_j,\ldots,X_nY_n)_B$=(01,…,01,…,01). This is a very important property since a checker is an embedded circuit whose input lines are not primary inputs of the

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chip. As a result, in most cases a checker receives during its normal, operation a predetermined set of codewords, which may be a subset of its entire input code space [15]. Thus, a usual problem in a checker design is that it must be testable with a reduced set of codewords. The above mentioned property of our checker makes it a suitable solution in cases with reduced input code space.

Finally, in order to provide the checker with the ability to "memorise" the error indication response on the outputs F and G, the modified, dual edge triggered Flip-Flop adopted in [11], along with the feedback technique proposed in [16], can be exploited. The self-testing ability of the extra hardware has been analysed in [13]. As it is shown in Fig. 4, nodes F and G are triggered on both edges of the clock signal *DCLK*, which is a delayed version of the system clock *CLK* by the response delay of the FSB or GSB sub-blocks plus the Flip-Flop's (MDFF) setup time. The two-railed outputs of the Flip-Flops are the Z_F and Z_G. The *RESET* signal is set initially to "1". In the fault free case the outputs Z_F and Z_G have complementary values. So the feedback mechanism does not interfere to the checker operation since at least one of the three serially connected pMOS or nMOS transistors are in the non-conducting state. In case of an error detection, Z_F and Z_G present equal values (either "0" or "1") so the corresponding triplet of serially connected transistors (pMOS or nMOS respectively) is set in the conducting state in both FSB and GSB forcing F and G permanently to the "high" state until the *RESET* signal is set to "0" for at least one clock period. In order to obtain the self-checking property of the "memorization" feedback circuitry, with respect to the TSOP faults, an extra stage is added to the CSR to generate the S_{zf} and S_{zg} control signals of Fig. 4.

4. Design issues and simulation results

The proposed parallel two-rail code checker (including the select signal generation circuitry) has been designed in a 0.18μm CMOS technology for a variety of *n*-variable values ranging from 32 to 256. The used power supply was 1.8V. The operation of our checker has been verified by SPICE simulations in all possible technology corners, for the fault free and all the possible faulty conditions in the checker according to the fault model discussed in Section 3, as well as for all possible types of erroneous input code words. Simulated waveforms are shown in Fig. 5.

For comparison reasons, the checker presented in [11] has been also designed for the same range of *n*-variable values. Both checkers have been optimized with respect to their response time. In Table I design issues and simulation results are presented for the two topologies. Initially, in columns 2 and 3 the implementation cost in unit size transistors (UST), considering various *n*-variable values for each design, is presented. As implementation cost in UST we define the number of minimum sized transistors, according to the used technology, that will cover the same area as the actual transistors in the design. Furthermore, in column 4 the cost reduction is given.

Next, comparisons based on simulation results between the two checkers are presented. The worst case response time (columns 5 and 6) and the power consumption in the fault free case (columns 8 and 9) are shown. The corresponding reductions are provided in columns 7 and 10. According to Table I, the proposed in this work checker is superior over the checker in [11] with respect to the required silicon area, the response delay time and the power consumption for high values of the *n*-variable.

Table I

Comparisons with respect to silicon area, response delay time and power consumption

Fan-In	Silicon Area Cost (UST)			Response Delay (ps)			Power Consumption (μW)		
	Proposed	**[11]**	**Reduction**	**Proposed**	**[11]**	**Reduction**	**Proposed**	**[11]**	**Reduction**
32	1012	304	-70.0%	440	620	29.0%	105.8	39.3	-62.8%
64	1822	1442	-20.8%	520	980	46.9%	123.4	85.2	-30.9%
128	3379	5757	41.3%	620	1710	63.7%	146.5	255	42.5%
256	6487	22025	70.5%	940	2992	68.6%	194.3	954	79.6%

The speed performance of the proposed checker stems from its current mode operation. The adopted current mirror topology is capable to provide fast sensing of the current flow through the array of the parallel connected pairs of transistors without the need for a full voltage swing on the internal nodes (N_F and N_G) of the checker as in the case of [11]. This way fast response times can be achieved with low silicon requirements, especially in the case of high *n*-variable values, since there is no need to fully charge/discharge the corresponding parasitic capacitances. Moreover, the reduced voltage swing on these nodes provides power savings in the case of large parasitic capacitances on these nodes (high *n*-variable values) despite the DC current path in each sub-block during the pertinent semi-period.

Finally, considering the noise sensitivity of the checker, we have to mention that its inputs are digital

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signals (not small analog signals) that are characterised by precisely defined noise margins. Since the checker does not need to detect small signal variations at its inputs, it is easy to design it not to be sensitive to the input noise.

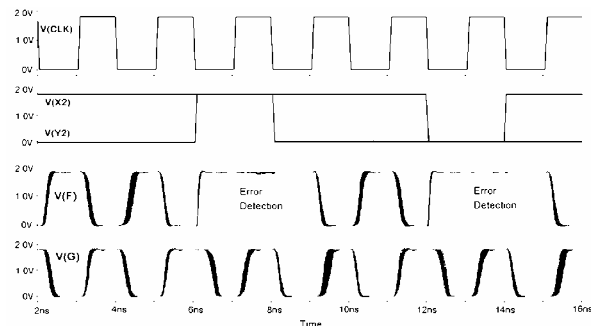

Figure. 5. Monte Carlo analysis waveforms (fan-in=64)

5. Conclusions

In this paper we presented a high speed and high testability, low cost parallel TRC checker suitable for the implementation of high fan-in circuits. The new checker belongs to the periodic outputs category of TRC checkers and it is TSC or SCD for a wide set of realistic faults, including TSOP faults that are not covered by other TRC checkers in the same class. Early simulations present a very high coverage also in the case of possible bridging faults up to 3KOhms.

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