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A Circuit for Concurrent Detection of Soft and Timing Errors in Digital CMOS ICs

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Abstract. In this paper a new circuit for concurrent soft and timing error detection in CMOS ICs is presented. The circuit is based on current mode sense amplifier topologies to provide fast error detection times. After an error has been detected it can be corrected by using a retry cycle.

Keywords: concurrent testing, soft and timing errors, monitoring circuits, time redundancy

1. Introduction

Progress in semiconductor technology poses new problems in IC design making difficult to achieve adequate reliability levels and keep the cost of testing within acceptable bounds. The device size scaling, the increased operating frequency and the power supply reduction that follow process scaling in modern technologies, affect circuit's noise margins and reliability. Under these circumstances the transient faults are becoming a major concern as they lead to increased and many times unacceptable soft error rate (SER) levels. Timing related transient faults due to crosstalk or ground bounce are well known mechanisms for soft error generation. In addition, single event upsets (SEUs) caused by cosmic-ray secondary neutrons and alpha particles emitted by impurities in electronic materials [5, 11, 12] seem that will play an important role to transient fault generation in future IC technologies.

The generated transient pulses (faults) on internal combinational logic nodes can propagate to the circuit outputs. These pulses are often attenuated before they reach an output. However, if they reach an output they may contribute to a soft error generation in

case they occur during the time at which the clock samples this output. This probability increases with the clock frequency. Therefore, in future technologies logic parts will require protection against soft errors analogous to this developed in the past for memories [8, 9].

Another important problem arises due to timing errors. Path delays are decreased and thus delay faults may result in timing errors that are not easily detectable (in terms of test cost) in high frequency and high device count ICs. The reason is that process variations and manufacturing defects affect circuit speed especially in nanometer technologies. The huge number of paths in modern circuits along with the complexity of testing may lead to a significant number of defective ICs that will pass the fabrication tests. Obviously, in both cases on-line testing techniques are becoming mandatory in order to achieve acceptable levels of soft and timing error robustness.

Duplication and triplication techniques are widely used to increase systems reliability. However, the extra cost, in power consumption and silicon area, related to the application of these techniques, makes them impractical for a wide variety of electronic circuits. Self-checking design is a possible candidate but depending on the circuit under consideration it may also require high hardware cost [2]. Recently, soft and/or timing error detection schemes have been proposed in the open literature [1, 2, 6, 7, 10, 13, 14] that are combined with a retry procedure after each error detection. These techniques are based on the temporal nature of the transient faults or the delayed response of timing faults to provide error tolerance using time redundancy. In that case timing errors are covered by applying a reduced clock frequency during the retry procedure.

In this paper we present a new soft and timing error detection circuit that delivers fast response times with the use of a current mode sense amplifier. Moreover, the time redundancy approach that has been adopted in recent works can be exploited to provide error tolerance in case that it will be combined with a retry cycle; that is, the correct result is obtained, each time an error is detected, by repeating the last operation using a lower frequency. The paper is organized as follows. In Section 2, the monitoring technique under consideration is presented and the new concurrent soft and timing error detection scheme is introduced and discussed. In Section 3, simulation results are provided in order to validate this approach and explore its feasibility. Finally, the conclusions are drawn in Section 4.

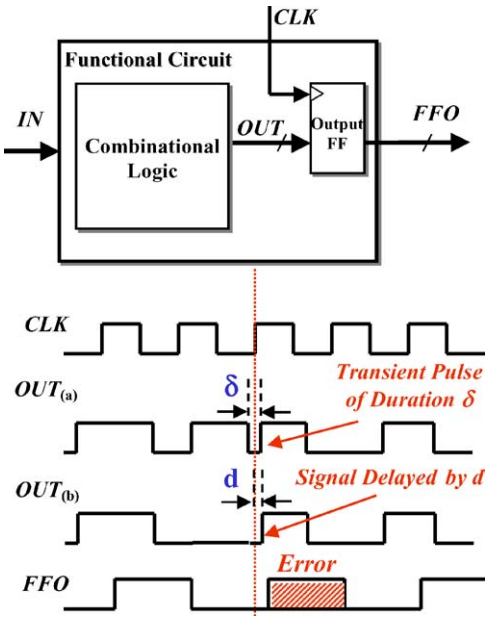

Fig. 1. Error generation mechanisms.

2. The Proposed Concurrent Error Detection Circuit

Fig. 1 presents a Functional Circuit consisting of the combinational part and the flip-flops of the output register. Transient faults on internal nodes of the combinational circuit may result in the appearance of transient pulses at its output lines *OUT*. In case that the triggering edge of the clock *CLK* arrives just after the transient pulse appearance and during its presence on the $OUT_{(a)}$ line (time interval δ), a soft error is generated at the output *FFO* of the flip-flop. Moreover, path delay faults in the combinational circuit may result in a delayed signal arrival at a circuit output $OUT_{(b)}$, after the triggering edge of the clock *CLK* (time interval d) and thus the generation of a timing error at the output *FFO* of the flip-flop.

The key idea behind the adopted error detection technique is the use of a Monitoring Circuit to monitor the responses at the outputs of the Combinational Circuit as well as the primary outputs of the Functional Circuit (see Fig. 2) after a time interval T from the latching edge of the clock signal *CLK* [1, 2, 6, 7, 10, 13, 14].

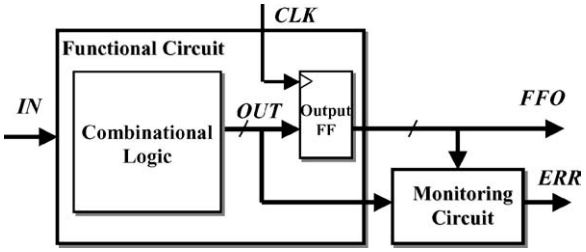

Fig. 2. Error detection using a monitoring circuit.

This time interval T is equal to the maximum value between the maximum transient pulse duration ($\delta_{\max}$) and the maximum signal delay time ($d_{\max}$), that must be detectable in order to achieve an acceptable error rate level ($T = \max[\delta_{\max}, d_{\max}]$).

In the fault free case no signal transitions appear on the monitored lines after the latching edge of the clock signal *CLK* (plus the flip-flop hold time) and the error indication signal of the Monitoring Circuit remains "low" (*ERR* = "low"). In the case that a transient or a delay fault in the combinational logic causes a transient pulse or a delayed signal response (transition) on the output line *OUT* of the Combinational Circuit when the latter is sampled by the clock *CLK*, the Output Flip-Flop captures an erroneous value and an error occurs (either soft or timing error respectively) on its output *FFO*. Then, after the expiration of the transient pulse duration time (δ) or after the signal delay time (d) the output line *OUT* turns to its correct value. The Monitoring Circuit detects the resulted difference between the values on the lines *OUT* and *FFO* and the error indication signal *ERR* rises to "high" (*ERR* = "high") indicating the error presence.

In this paper we propose a new Monitoring Circuit that exploits sense amplifier based signal amplification techniques for soft and timing error detection. Sense amplifiers are widely used in semiconductor memories to retrieve the data stored in a memory array by amplifying small signal variations on their inputs. They can provide fast response times under large loads on their input lines. The proposed Monitoring Circuit is shown in Fig. 3 and consists of a Sense Amplifier (SA), a Pre-Sensing Block (PSB) and an Error Indication Flip-Flop (EIFF). The Pre-Sensing Block is divided into two sub-blocks (SBL and SBR) each one feeding a separate input of the sense amplifier *INL* and *INR* respectively. The k pairs of monitored lines OUT_j and FFO_j ($j \in [1 .. k]$), are driving both sub-blocks of the Pre-Sensing Block. Each sub-block consists of $2k$ pairs of serially connected nMOS transistors. In the left sub-block SBL the $2k$ pairs of transistors are connected in parallel between the V_{DD} power supply (through an nMOS transistor—MFL) and the left input of the sense amplifier *INL*. Each pair is driven by a distinct combination of monitored signals in such a way that for every pair of monitored lines (OUT_j and FFO_j) there exist two pairs of transistors where the one is driven by the signals OUT_j and $\overline{FFO_j}$ and the other

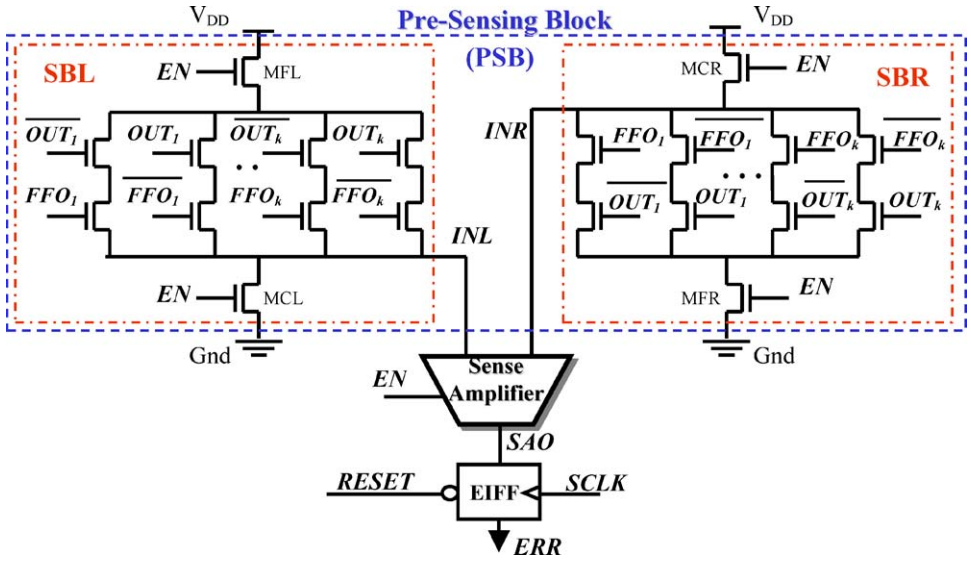

Fig. 3. The proposed monitorting circuit.

by the signals $\overline{OUT_j}$ and FFO_j. The transistor MFL is driven by the enable signal *EN*. In addition a single nMOS transistor (MCL) is connected between the Gnd power supply and the left input of the sense amplifier and it is also driven by the enable signal *EN*. Each path formation between the power supply V_{DD} and *INL* through MFL and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCL. In the right sub-block SBR a quite similar topology is present. An identical arrangement of $2k$ pairs of transistors exists, where each pair of transistors is connected between the Gnd power supply (through an nMOS transistor—MFR) and the right input of the sense amplifier *INR*. These pairs are driven in exactly the same way as in the case of the left sub-block. The MFR transistor is driven by the *EN* signal. Finally, a single nMOS transistor (MCR) is connected between the V_{DD} power supply and the right input of the sense amplifier and it is also driven by the *EN* signal. Again, each path formation between the power supply Gnd and *INR* through MFR and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCR.

The Sense Amplifier is activated by the *EN* signal and provides the output signal *SAO*, which is latched by the Error Indication Flip-Flop at the rising edge of signal *SCLK*. The signal *SCLK* is identical to the signal *CLK* but shifted by a time interval equal to $T+D_{SA}$, where D_{SA} is the sensing delay of the Sense Amplifier.

Initially, at the system power-up the Error Indication Flip-Flop is set to "low" (*ERR* = "low") using the *RESET* signal. Then, during the system operation each period of the clock *CLK* can be seen as divided in two phases, the normal phase and the monitoring phase, which are defined by the *EN* signal, as it is shown in Fig. 4. These phases are transparent to the Functional Circuit under monitoring. In the normal phase, the Monitoring Circuit is inactive (*EN* = "low"). After the rising edge of *CLK* that captures the response of the combinational logic in the Output Flip-Flop the signal *EN* is set to "high" to activate the monitoring mechanism (monitoring phase). The time difference (T) between the rising (triggering) edge of signal *CLK* and the rising edge of signal *EN* is equal to the maximum of the time durations δ_{max} and d_{max} that are required to be detectable. The time T must also be greater than the Output Flip-Flops' hold time, in order that the signals on the FFO_j lines are stable but this is always true since δ_{max} and d_{max} are greater than a flip-flop's hold time. Moreover, the *EN* signal is active ("high") for a time interval equal to the sensing delay D_{SA} of the Sense Amplifier. Finally, the signals on the *OUTj* lines must be stable, in the error free case, for a time interval equal

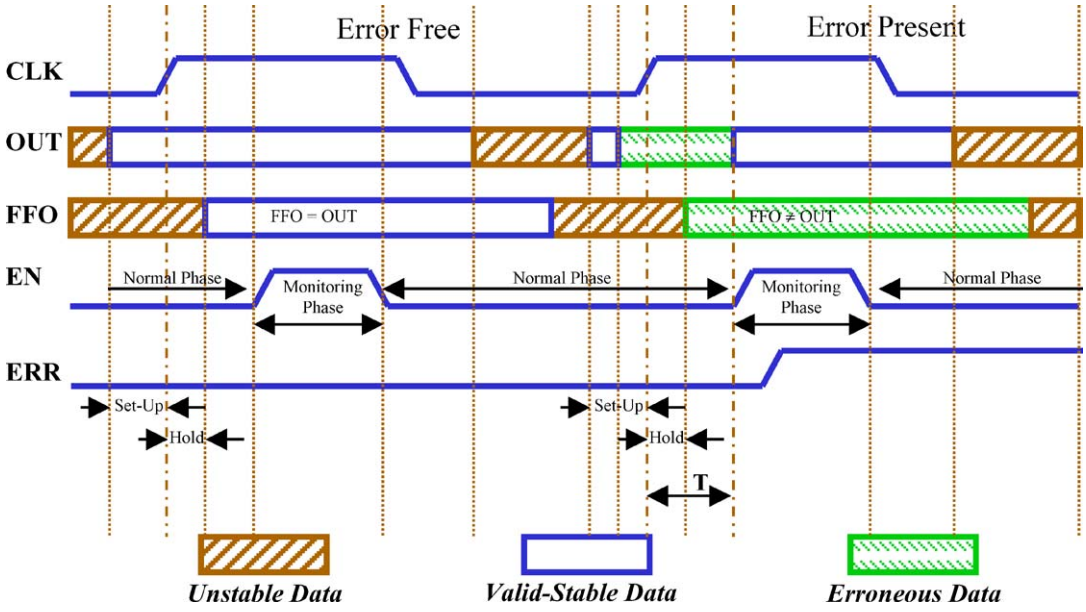

Fig. 4. Signals' timing for the monitorting circuit.

to $T+D_{SA}$ after the triggering edge of the clock to avoid false alarms.

In the error free case where $OUT_j = FFO_j$ ($\forall j \in [1..k]$) during the monitoring phase, there is no current path formation in the Pre-Sensing Block between the lines *INL* and *INR* and the power supplies V_{DD} and Gnd respectively. Thus, the input *INL* of the Sense Amplifier is discharged through the transistor MCL with a current $-I_L = I_{MCL} < 0$, while the input *INR* is charged through the transistor MCR with a current $I_R = I_{MCR} > 0$. Currents $-I_L$ and I_R generate a current difference $\Delta I = -I_L - I_R = -(I_L + I_R) < 0$ at the input terminals of the Sense Amplifier. The Sense Amplifier will amplify this signal difference driving fast its output *SAO* to "low".

In the presence of an error, there exists at least one pair of monitored lines such that $OUT_j \neq FFO_j$ ($j \in [1..k]$). Thus, there will be at least one current path formation between *INL* and V_{DD} through transistor MFL (I_{MFL}), as well as a current path formation between *INR* and Gnd through transistor MFR (I_{MFR}). Since the established current paths are dominant compared to the current paths through transistors MCL and MCR respectively ($I_{MFL} \gg I_{MCL}$ and $I_{MFR} \gg I_{MCR}$), the input line *INL* of the Sense Amplifier is charged with a current $I_L = I_{MFL} - I_{MCL} > 0$, while the input line *INR* is discharged with a current $-I_R = -I_{MFR} + I_{MCR} = -(I_{MFR} - I_{MCR}) < 0$. Currents I_L and $-I_R$ provide a current difference $\Delta I = I_L - (-I_R) = I_L + I_R > 0$ at the input terminals of the Sense Amplifier. In that case, the Sense Amplifier will amplify this opposite signal difference driving fast its output *SAO* to "high". This response is latched by the Error Indication Flip-Flop at the rising edge of *SCLK* turning signal *ERR* to "high" and providing the indication of an error detection. The *ERR* line remains "high" until the *RESET* signal is activated after the proper actions of the system to handle the erroneous situation (retry procedure).

Note that in contradistinction to the operation of the current mode sense amplifiers used in memories where current differences ΔI are small signals (due to the use of small transistor sizes for high-density reasons), in our case these current differences can be quite large signals with proper selection of the transistor sizes in the PSB.

The contribution of this work stems from the fact that, since the Sense Amplifier is characterized by very small sensing delays D_{SA}, the proposed monitoring circuit is capable to provide very fast responses compared to other monitoring techniques in the literature. Thus, it can be exploited in high performance applications where the monitoring phase must be a small portion of the clock period, in order to be completed before the *OUT* lines turn into an unstable state.

Finally, we have to mention that in the case of soft errors for which a transient pulse appears on an output line *OUT* after the triggering edge of the clock, a false error detection alarm will be flagged by the monitoring circuit although the value latched on the line *FFO* of the Output Flip-Flop is correct. This is a known problem for all monitoring circuits of this kind in the open literature. However, this will not affect the correct operation of the circuit, neither the overall system performance, since the speed degradation is expected to be one lost operating cycle in a very large number of system operating cycles, while it is guaranteed that every soft error that must be detected will be detected.

3. Circuit Design and Simulation Results

In the design of the Monitoring Circuit presented in the previous section, the current mode, self-precharged Sense Amplifier of Fig. 5, proposed in [3], which provides extremely small sensing delay times, has been used. The main characteristic of this circuit is that its response times are almost independent of the capacitance load on its inputs [4]. The Sense Amplifier operates in two phases, the precharge/equalization and the sensing. A precharge/equalization phase always precedes a

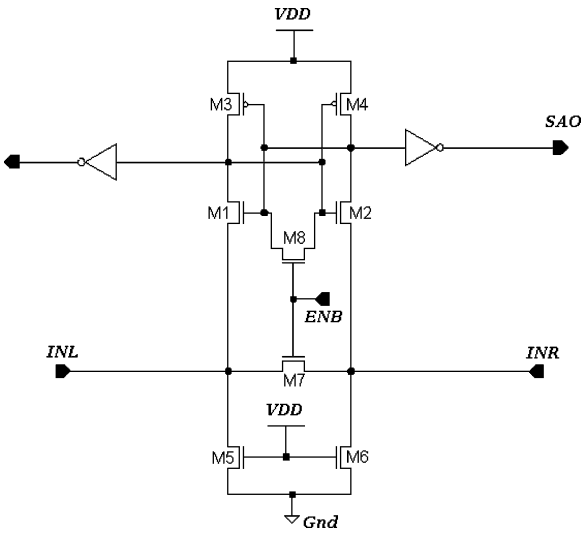

Fig. 5. The sense amplifier.

sensing phase and is used to set the internal nodes of the Sense Amplifier to proper voltage levels as well as to equalize the voltage level on its inputs. The Sense Amplifier under consideration is a self-precharged circuit and thus there is no need for any dedicated precharge circuitry or any extra voltage source. During the time period where *EN* = "low" the Sense Amplifier is in the precharge/equalization phase and the transistors M7 and M8 are "on" to equalize the voltage levels between the lines *INL* and *INR* as well as the output lines of the cross-coupled pair M1–M4. These two transistors must be quite large for fast equalization. The sensing phase is activated when *EN* = "high" and is identical to the monitoring phase of the Monitoring Circuit. Transistors M7 and M8 are turned off, and the cross-coupled transistor structure M1–M4 acts as a high-gain positive feedback amplifier. Since the PSB is active during this period, the transistors M1 and M2 begin to source the current provided by SBL and SBR respectively. The difference current ΔI flowing through M1 and M2 provides a voltage difference rise across the output nodes (drain nodes of M1 and M2) of the Sense Amplifier. This initially increasing voltage difference is rapidly amplified by the positive feedback of the structure, driving the left output to "high" and the right output to "low" for the case of a positive ΔI or to the complementary states in the opposite case.

Since the Pre-Sensing Block has been designed with the use of only nMOS transistors, the Monitoring Circuit presents a very stable behaviour under process variations. However, pMOS transistors can be used for MFL and MCR without any drawbacks in the circuit operation. Furthermore, considering the topology configuration of Fig. 3, the parasitic capacitances seen at the inputs *INL* and *INR* of the Sense Amplifier are always equal for both the error free and the erroneous cases independently of the input combinations (signals OUT_j and FFO_j) of the Pre-Sensing Block. Thus, the voltage on these lines can be easily equalized (by activating transistor M7) during the precharge/equalization phase and the Sense Amplifier is always balanced when entering the sensing phase.

The 0.18 μm CMOS technology of ST Microelectronics with 1.8 V power supply has been exploited for the design of the proposed error Monitoring Circuit. As an example we will consider the case of 72 monitored pairs. Optimising the design with respect to speed performance the following transistor sizes were selected. In the Pre-Sensing Block the transistor aspect ratios used were: W/L = 4 for the pairs of transistors driven by the monitored pairs of lines OUT_j and FFO_j, W/L = 28 for the MFL and MFR transistors and W/L = 0.3 for the MCL and MCR transistors. The aspect ratios of the transistors used in the Sense Amplifier of Fig. 5 were: W/L = 2 for the transistors M1 and M2, W/L = 8 for M3 and M4, W/L = 0.33 for M5 and M6, W/L = 40 and W/L = 10 for the transistors M7 and M8 respectively. The layout design of the proposed circuit is given in Fig. 6. The "folded bit-line" design technique, which is commonly used in memory array design, is exploited in order to achieve a high density Pre-Sensing Block and make the Monitoring Circuit insensitive to process and temperature variations.

The simulated waveforms of the signals *EN*, *OUT* and *FFO* as well as the response signal *SAO* of the Sense Amplifier are presented in Fig. 7 for the case of 72 monitored pairs and for typical transistor models in 27°C. The clock period is 1 ns. The upper curves of the above figure show the signals *OUT* and *FFO* of the Functional Circuit under monitoring, while in the

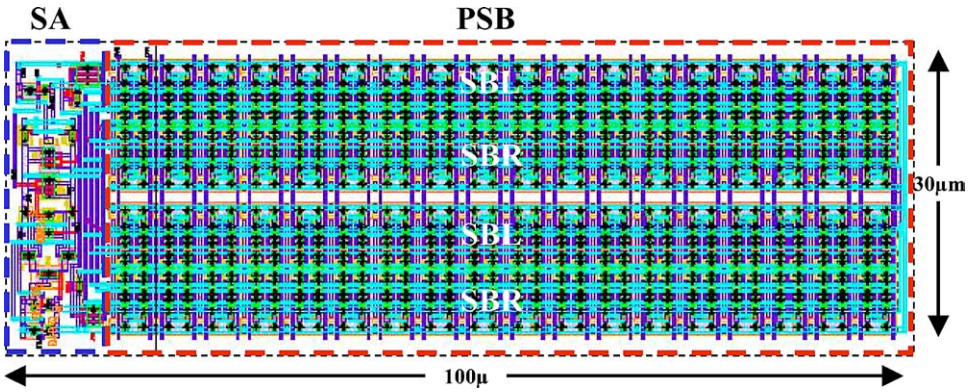

Fig. 6. Layout of the Monitoring Circuit for 72 monitored pairs of lines.

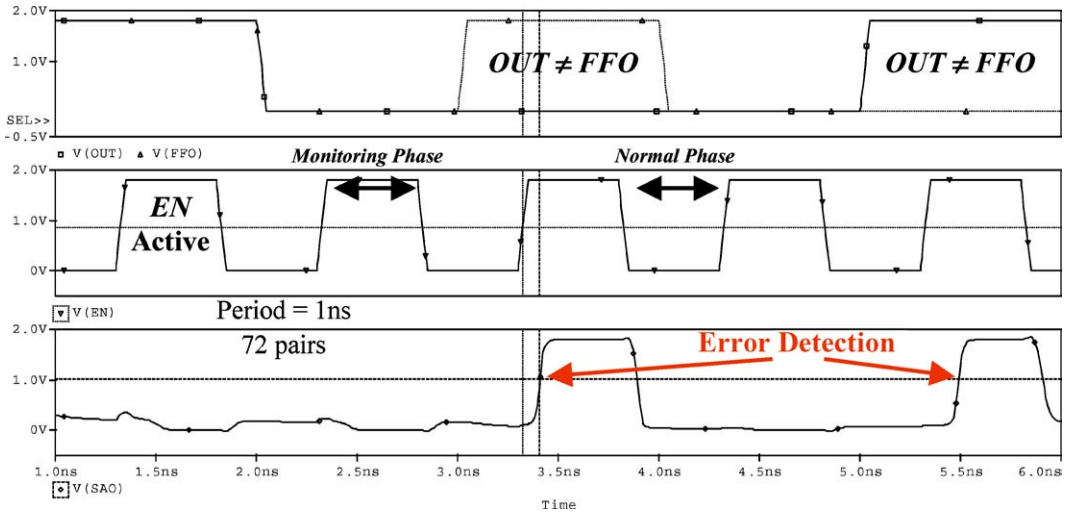

Fig. 7. Simulated waveforms.

middle curve the waveform of the *EN* signal is drawn. Finally, the lower curve shows the response (pass/fail) signal *SAO* of the Sense Amplifier. Five cases are presented. In the first two and the fourth both signals *OUT* and *FFO* have equal values (either high or low), during the time interval of the monitoring phase, while in the third and fifth the two signals are complementary (*OUT* = "low", *FFO* = "high" and *OUT* = "high", *FFO* = "low" respectively) representing an erroneous state when the *EN* signal is activated. Only in the latter cases the output of the Sense Amplifier turns "high", just after the enable signal *EN* goes active ("high"), indicating the detection of the error. In addition, Monte Carlo simulations considering parameter statistical variations up to 20% have been carried out (see Fig. 8) in order to explore the circuit behavior under mismatches in the MOS devices. In all cases the circuit response was the proper one. Finally, the power consumption of the monitoring circuit was equal to 0.38 mW.

Similar simulations have been carried out for various numbers of monitored pairs (from 9 to 576), for temperatures up to 125°C, voltage variations in the range of ±10% and using all process corner conditions for the MOS transistors in the design. In all combinations

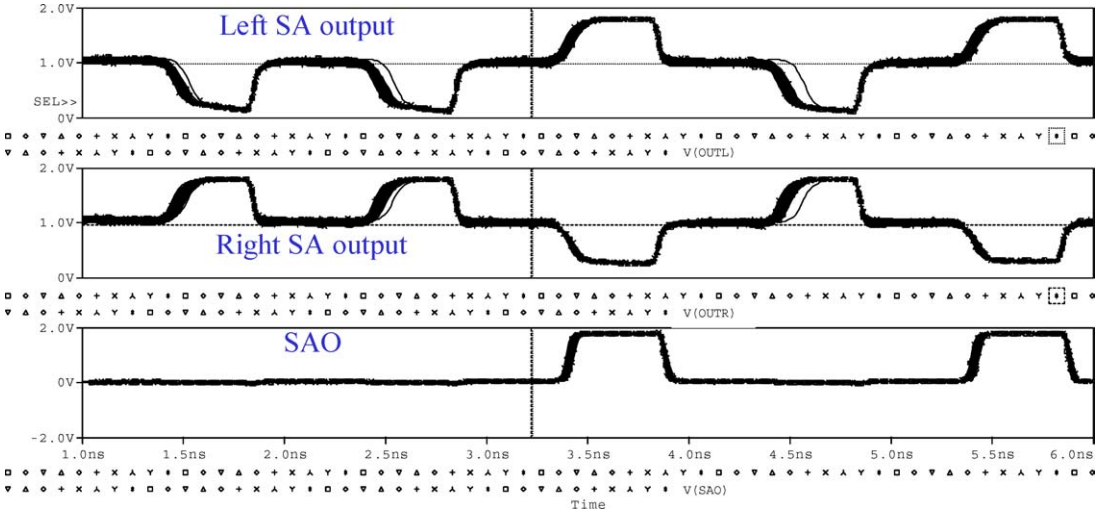

Fig. 8. Monte Carlo Simulations.

Table 1. Detection time comparisons.

Number of monitored pairs	Detection time (ps)		Reduction (%)
	[13]	Proposed	
9	456	191	58
18	501	226	55
36	581	265	54
72	721	317	56
144	979	376	62
288	1485	430	71
576	2480	468	81

of PVT (process-voltage-temperature) conditions the circuit operation was the proper one. Table 1 provides comparisons between the detection times reported for a fast monitoring circuit presented in [13] and the corresponding times in this work, with respect to the number of monitored pairs. The detection time is defined as the time interval between the activation of the *EN* signal and the response of the Monitoring Circuit. These measurements have been carried out at 125°C and for the slow-slow transistor model, which, according to the simulations, provide the worst-case response times. In Fig. 9, a graphical representation of the values in Table 1 is given. As it is shown, for large numbers of monitored pairs the detection time of the present circuit comes to saturation due to the low sensitivity of the selected Sense Amplifier to the input capacitance load, while the circuit in [13] has a linear dependence to this load. The new monitoring circuit is expected to be much faster than the corresponding circuit presented in [2], since, especially for large numbers of monitored pairs, the latter requires a quite large number of logic

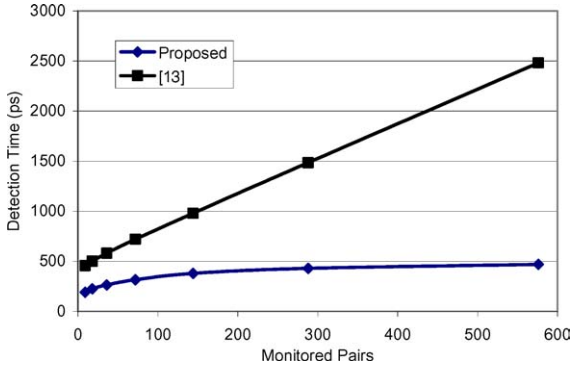

Fig. 9. Detection time vs. the number of monitored pairs.

levels to provide its response. Moreover, the silicon area requirements of our circuit are comparable to these of the circuit in [2], but both present a much higher area cost than that in [13].

4. Conclusion

In this paper, a novel monitoring circuit for the concurrent detection of soft and timing errors in CMOS ICs is presented. It uses a sense amplifier to detect the erroneous responses at the outputs of the functional circuit being monitored. The adopted approach can deliver very fast detection times compared to techniques presented earlier in the literature. The existing and mature technology of embedded SRAMs can provide all the necessary solutions for the robust and reliable design of the proposed monitoring circuit, while the use of parametric circuit generators like these exploited in memory design can automate its design. Finally, combining the proposed monitoring circuit with a retry procedure, error tolerance can be achieved.

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