A Sense Amplifier Based Circuit for Concurrent Detection of Soft and Timing Errors in CMOS ICs

Y. Tsiatouhas[1], S. Matakias[2], A. Arapoyanni[2] and Th. Haniotakis[3]

[1]University of Ioannina, Dept. of Computer Science, P.O. Box 1186, 45110 Ioannina, Greece
[2]University of Athens, Dept. of Informatics & Telecom., Panepistimioupolis, 15784 Athens, Greece
[3]Southern Illinois University, Dept. of Electrical & Computer Engineering, 62901 Carbondale, USA
e-mails: tsiatouhas@cs.uoi.gr, {s.matakias, arapoyanni}@di.uoa.gr, haniotak@siu.edu

Abstract

We propose a new concurrent soft and timing error detection circuit that exploits the time redundancy approach to achieve tolerance with respect to transient and delay faults. The idea is based on current mode sense amplifier topologies to provide fast error detection times.

1. Introduction

Progress in technology poses new problems in IC design making difficult to achieve adequate reliability levels and keep the cost of testing within acceptable bounds. The device size scaling, the increased operating frequency and the power supply reduction that follow process scaling in modern technologies, affect circuit's noise margins and reliability. Under these circumstances the transient faults are becoming a major concern as they lead to increased and many times unacceptable soft error rate (SER) levels. Timing related transient faults due to crosstalk or ground bounce are well known mechanisms for soft error generation. In addition, single event upsets (SEUs) caused by cosmic-ray secondary neutrons and alpha particles emitted by impurities in electronic materials [1-4] seem that will play an important role to transient fault generation in future IC technologies.

The transient pulses (faults) generated on internal combinational logic nodes can propagate inside the circuit. These pulses are often attenuated before they reach an output. Furthermore, even if they reach an output they will contribute to a soft error generation only if they occur during the time at which the clock samples this output. However, since the duration of the clock cycle decreases, the probability that the transient pulse is captured by the clock edge increases. Therefore, in future technologies logic parts will require protection against soft errors analogous to this developed earlier for memories [5-6].

In addition to the previous situation another important problem arises due to timing errors. Path delays are increased and may result in timing errors that are not easily detectable (in terms of test cost) in high frequency and high device count ICs. The reason is that process variations and manufacturing defects affect circuit speed especially in nanometer technologies. The huge number of paths in modern circuits along with the complexity of testing may lead in a significant number of defective ICs that will pass the fabrication tests. Obviously, in both cases on-line testing techniques are becoming mandatory in order to achieve acceptable levels of soft and timing error robustness.

Duplication and triplication techniques are widely used to achieve systems reliability. However, the extra cost, in power consumption and silicon area related to the application of these techniques, makes them impractical for a wide variety of electronic circuits. As an alternative approach, concurrent checking schemes combined with a retry procedure after each error detection can be considered. Timing errors can also be covered applying a reduced clock frequency during the retry procedure. Self-checking design is a possible candidate but depending on the circuit under consideration it may also require high hardware cost [11]. Recently, soft and/or timing error detection techniques have been proposed in the open literature [7-13] that are based on the temporal nature of the transient faults or the delayed response of timing faults to provide error tolerance using time redundancy.

In this paper, we present a new soft and timing error detection circuit. It exploits the time redundancy approach that has been adopted in recent works and provides error tolerance in case that it will be combined with a retry cycle; that is, each time an error is detected the correct result is obtained by repeating the last operation using a lower frequency. The paper is organized as follows. In section 2 the time redundancy technique is presented and the new concurrent soft error detection scheme is introduced and discussed. In section 3 simulation results are provided in order to validate this approach and explore its feasibility in future technologies. Finally, the conclusions are drawn in section 4.

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2. A novel concurrent error detection circuit

Fig. 1 presents a Functional Circuit consisting of the combinational part and the flip-flops of the output register. Transient faults on internal nodes of the combinational circuit may result in the appearance of transient pulses at its output lines *OUT*. In case that the triggering edge of the clock *CLK* arrives just after the transient pulse appearance and during its presence on the *OUT* line (time interval δ), a soft error is generated at the output *FFO* of the flip-flop. Moreover, path delay faults in the combinational circuit may result in a signal arrival at the circuit outputs after the triggering edge of the clock *CLK* and thus the generation of a timing error at the output *FFO* of the flip-flop.

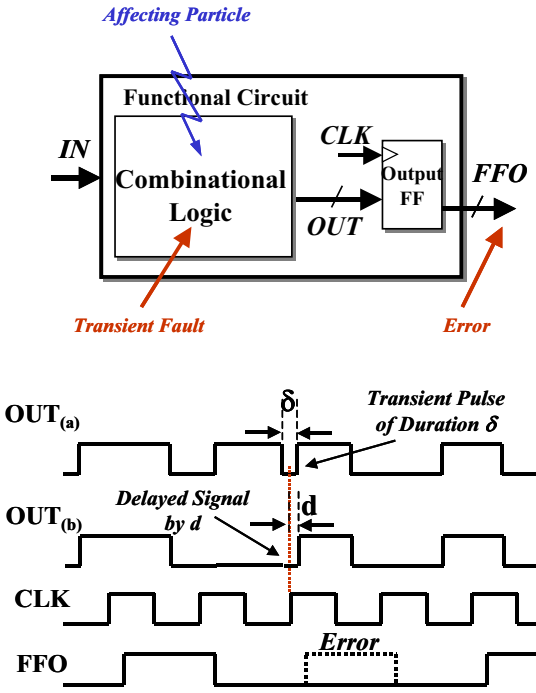

Figure 1: Error generation mechanisms

The key idea behind the time redundancy based error detection technique is the use of a Monitoring Circuit to monitor the responses at the outputs of the Combinational and Functional Circuits (see Fig. 2) for a time interval T after the latching edge of the clock signal *CLK* [7-13]. The time interval T depends on either the maximum transient pulse duration (δ_{max}) or the maximum signal delay time (d_{max}) that must be detectable in order to achieve an acceptable error rate level.

In the fault free case no signal transitions appear on the monitored lines after the latching edge of the clock signal *CLK* and the error indication signal of the Monitoring Circuit remains "low" (*ERR*="low"). In the case that a transient or a delay fault in the combinational logic causes a transient pulse or a delayed signal response (transition) on the output line *OUT* of the Combinational Circuit when the latter is sampled by the clock *CLK*, the Output Flip-Flop captures an erroneous value (see Fig. 1(b)) and an error occurs (either soft or timing error respectively) on its output *FFO*. Then, after the expiration of the transient pulse duration time (δ) or after the signal delay time (d), the output line *OUT* turns to its correct value. The Monitoring Circuit detects this transition and the error indication line *ERR* rises to "high" (*ERR*="high") indicating the error presence.

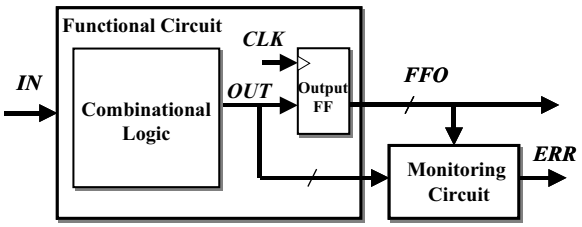

Figure 2: The error detection technique based on time redundancy

In this paper we propose a new Monitoring Circuit for soft and timing error detection that is originated from sense amplifier based signal amplification techniques. Sense amplifiers are widely used in semiconductor memories to retrieve the stored data in a memory array by amplifying small signal variations on their inputs. They can provide fast response times under large loads on their input lines. The proposed Monitoring Circuit is shown in Fig. 3 and consists of a Sense Amplifier (SA), a Pre-Sensing Block (PSB) and an Error Indication Flip-Flop (EIFF). The Pre-Sensing Block is divided into two sub-blocks (SBL and SBR) each one feeding a separate input of the sense amplifier *INL* and *INR* respectively. The k pairs of monitored lines OUT_j and FFO_j ($j \in [1 .. k]$), are driving both the sub-blocks of the Pre-Sensing Block. Each sub-block consists of 2k pairs of serially connected nMOS transistors. In the left sub-block the 2k pairs of transistors are connected in parallel between the V_{DD} power supply (through an nMOS transistor - MFL) and the left input of the sense amplifier. Each pair is driven by a distinct combination of monitored signals in such a way that for every pair of monitored lines (OUT_j and FFO_j) there exist two pairs of transistors where the one is driven by the signals OUT_j and $\overline{FFO_j}$ and the other by the signals $\overline{OUT_j}$ and FFO_j. The transistor MFL is driven by the enable signal, *EN*. In addition a single nMOS transistor (MCL) is connected between the Gnd power supply and the left input of the sense amplifier and is also driven by the enable signal, *EN*. Each path formation

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between the power supply V_{DD} and *INL* through MFL and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCL. In the right sub-block a quite similar topology is present. An identical arrangement of 2k pairs of transistors are connected between the Gnd power supply (through an nMOS transistor - MFR) and the right input of the sense amplifier. Each pair is driven in exactly the same way as in the case of the left sub-block. The MFR transistor is driven by the *EN* signal. Finally, a single nMOS transistor (MCR) is connected between the V_{DD} power supply and the right input of the sense amplifier and is also driven by the *EN* signal. Again, each path formation between the power supply Gnd and *INR* through MFR and a pair of transistors is designed to be more conductive (dominant) than the single transistor MCR.

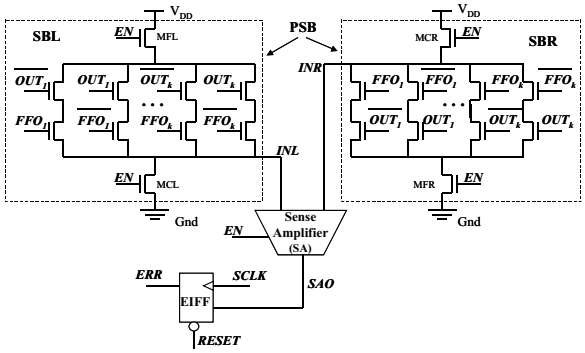

Figure 3: The proposed Monitoring Circuit

The Sense Amplifier is activated by the *EN* signal and provides the output signal *SAO*, which is latched by the Error Indication Flip-Flop at the rising edge of signal *SCLK* that is a shifted version of *CLK* by a time interval equal to $\delta_{max}+D_{SA}$ or $d_{max}+D_{SA}$ where D_{SA} is the sensing delay of the Sense Amplifier.

Initially, at the system power-up the Error Indication Flip-Flop is preset to "low" (*ERR*="low") using the *PRESET* signal. Then, during the system operation each period of the clock, *CLK*, can be seen as divided in two phases, the normal phase and the monitoring phase, which are discriminated by the *EN* signal, as it is shown in Fig. 4. These phases are transparent to the Functional Circuit under monitoring. In the normal phase, the Monitoring Circuit is inactive (*EN*="low"). After the rising edge of *CLK* that captures the response of the combinational logic in the Output Flip-Flop the signal *EN* is set to "high" to activate the monitoring mechanism (monitoring phase). The timing difference between the rising edges of the *CLK* and the *EN* signals is equal to the maximum value among the maximum transient pulse duration (δ_{max}) and the maximum signal delay time (d_{max}), which are required to be detected. Moreover, the *EN* signal remains "high" for at least a time interval equal to the sensing delay D_{SA} of the Sense Amplifier.

In the error free case where $OUT_j = FFO_j$ ($\forall$ j$\in$[1 .. k]) during the monitoring phase, there is no path formation between the inputs *INL* and *INR* of the Sense Amplifier and the power supplies V_{DD} and Gnd respectively, through the Pre-Sensing Block. Thus, the input *INL* of the Sense Amplifier is discharged through the transistor MCL while the input *INR* is charged through the transistor MCR. The Sense Amplifier will amplify the signal difference between its two inputs driving fast its output *SAO* to "low".

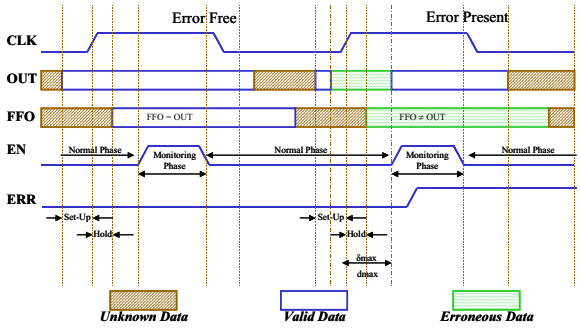

Figure 4: Signal timing for the proposed Monitoring Circuit

In the presence of an error there exists at least one pair of monitored lines such that $OUT_j \neq FFO_j$ (j$\in$[1 .. k]). Thus, there will be at least one path formation between *INL* and V_{DD} as well as a path formation between *INR* and Gnd. Since the established paths are dominant compared to the paths through transistors MCL and MCR respectively, the input *INL* of the Sense Amplifier is charged while the input *INR* is discharged. Also in that case, the Sense Amplifier will amplify the signal difference between its inputs driving fast its output *SAO* to "high". This response is latched by the Error Indication Flip-Flop at the rising edge of *SCLK* turning signal *ERR* to "high" and providing the indication of an error detection. The *ERR* line remains "high" until the *PRESET* signal is activated after the proper actions of the system to handle the erroneous situation.

3. Circuit design and simulation results

In the design of the Monitoring Circuit presented in the previous section, the current mode, self-precharged Sense Amplifier proposed in [14] has been used, which provides extremely small sensing delay times. The main characteristic of this circuit is that its response times are almost independent of the load capacitance on its inputs [15]. The Sense Amplifier operates in two phases, the precharge/equalization and the sensing. A precharge/equalization phase always precedes a sensing phase and is used to set the internal nodes of the Sense

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Amplifier to proper voltage levels as well as to equalize the voltage level on its inputs. The Sense Amplifier under consideration is a self-precharged circuit and thus there is no need for any dedicated precharge action or any extra voltage source. During the time period where *EN*="low" the Sense Amplifier is in the precharge/equalization phase. The sensing phase is activated when *EN* ="high" and is identical to the monitoring phase of the Monitoring Circuit.

Since the Pre-Sensing Block has been designed with the use of only nMOS transistors, the Monitoring Circuit presents a very stable behaviour under process variations. Furthermore, considering the topology configuration of Fig. 3, the parasitic capacitances seen at the inputs *INL* and *INR* of the Sense Amplifier are always equal for both the error free and the erroneous cases independently of the possible input combinations (signals OUT_j and FFO_j) of the Pre-Sensing Block. Thus, the voltage on these lines can be easily equalized during the precharge /equalization phase and the Sense Amplifier is always balanced when entering the sensing phase. Layout design techniques like these commonly used in memory array design (folded bit-lines etc) can be exploited in order to achieve a high density Pre-Sensing Block and improve further the behaviour of the Monitoring Circuit making it tolerant in process and temperature variations.

The 0.18μm CMOS technology of ST Microelectronics with 1.8V power supply has been exploited for the design of the proposed error Monitoring Circuit. As an example we will consider the case of 72 monitored pairs. In the implementation of the Pre-Sensing Block the following transistor aspect ratios have been used: W/L = 4 for the pairs of transistors driven by the monitored pairs of lines OUT_j and FFO_j, W/L = 28 for the MFL and MFR transistors and W/L = 0.3 for the MCL and MCR transistors.

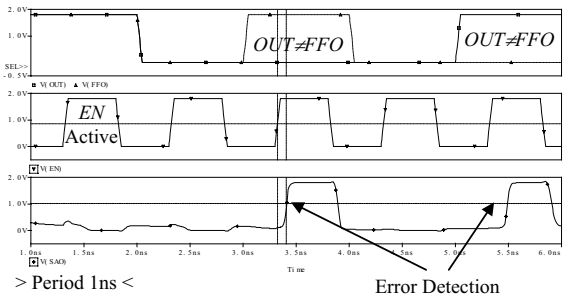

Figure 5: Simulated waveforms

The simulated waveforms of the signals *EN*, *OUT* and *FFO* as well as the response signal *SAO* of the Sense Amplifier are presented in Fig. 5, for the case of 72 monitored pairs and for typical transistor models in 27° C. The upper curves of Fig. 5 show the signals *OUT* and *FFO* of the Functional Circuit under monitoring, while in the middle curve the waveform of the *EN* signal is drawn. Finally, the lower curve shows the response (pass/fail) signal *SAO* of the Sense Amplifier. Five cases are presented. In the first two and the fourth, during the time interval of the monitoring phase, both signals *OUT* and *FFO* have equal values (either high or low) while in the third and fifth the two signals are complementary (*OUT*="low", *FFO*="high" and *OUT*="high", *FFO*="low" respectively). Only in the latter cases the output of the Sense Amplifier turns "high", just after the enable signal *EN* goes active ("high"), indicating the detection of the error.

Table I

Implementation cost and detection time of the proposed scheme

Number of Monitored Pairs	Implementation Cost in Unit Transistors (ut)	Worst Case Detection Time (ps)
9	290	191
18	491	226
36	894	265
72	1701	317
144	3314	380
288	6539	430
576	12990	470

Similar simulations have been carried out for various numbers of monitored pairs (from 9 to 576), for temperatures equal to 27° C and 125°C and using slow, typical and fast transistor models as well as their combinations for the pMOS and the nMOS transistors of the design. Table I presents the implementation cost in unit transistors (ut) and the worst case detection time of the proposed Monitoring Circuit for indicative numbers of monitored pairs. As a unit transistor we consider a minimum size transistor. The cost of the Sense Amplifier is equal to 52 unit transistors. Moreover, the detection time has been measured at 125°C and for the slow-slow transistor model (SS), which according to the simulations provides the worst case response time. In the curve of Fig. 6 the detection time of the Sense Amplifier with respect to the number of monitored pairs is illustrated. As it is shown, for large numbers of monitored pairs the curve comes to saturation due to the low sensitivity of the selected Sense Amplifier to the input load.

4. Conclusions

In this paper we presented a novel monitoring circuit for concurrent detection of soft and timing errors in CMOS ICs that is based on the use of fast sense amplifiers. The circuit exploits the temporary nature of the transient faults as well as the delayed response of the delay faults to detect the corresponding errors that appear at the outputs of the Functional Circuit being monitored.

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Then a retry procedure can be applied in order to restore the correct responses.

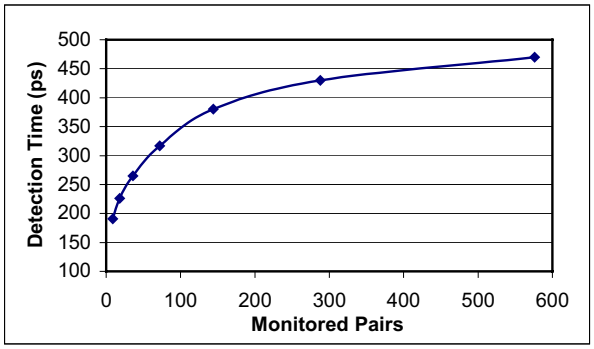

Figure 6: Detection time vs number of monitored pairs

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