DESIGN AND IMPLEMENTATION OF AN OPTO-ELECTRONIC TRANSCEIVER FOR OPTICAL FIBER COMMUNICATION OF MULTIPLEXED ANALOG VOICE, DIGITAL DATA AND VIDEO SIGNAL

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Abstract. In this paper an optimised design and the corresponding prototype of an opto-electronic transceiver for simultaneous analog and digital signal communication through optical fiber, are presented. The main functions of the transceiver are: a) to multiplex the analog audio signal (voice grade channel 300 to 3400Hz), serial data (R5232, 19.2kbps) and video data streams (compressed MPEG-I), b) to frame and transmit over an optical fiber the resulting stream in one direction, and c) to simultaneously and independently decode and de-multiplex the received optical data stream of the opposite direction. The system uses a micro-controller and a special designed ASIC to perform the multiplexing and de-multiplexing of the three different data sources.

Keywords. Fiber Optics, Communications, MPEG-1, Video Transmission, Multiplexing, De-multiplexing, E1 encoder, E1 decoder, Clock recovery.

GENERAL

The FOVIT system was designed to perform a simple fiber optic link between two points. It can transmit and receive simultaneously and independently through simple optical fiber three different signals.

1. a voice channel with analog bandwidth of 3.5KHz or 64 Kbits/sec stream of PCM encoded digital signal
2. a 2.048 Mbit/sec stream of E1 encoded video data and
3. a 19.2 Kbits/sec RS232 serial port for connection with a PC

The FOVIT-ASIC chip performs all the basic functions. The Figure 1 shows the connections between the FOVIT, the fiber optic link and the peripherals. Also, some additional circuits are included providing the interface between the E1 line coded data, the clock extraction, the line clock generation and the voice signal conversion. Figure 2 shows a more detailed diagram between the ASIC and the necessary ICs.

1. BASIC MODULES OF THE FOVIT ASIC

The main function of the FOVIT ASIC is to multiplex the audio and video streams then frame and transmits the resulting stream in one direction and simultaneously and independently decodes and de-multiplexes the received data stream in the opposite direction. In addition the ASIC provides a microprocessor interface witch will be used for communications with an external micro-controller.

The ASIC was designed using hierarchical design. The core block is consisted of the

transmitter, the receiver and the microcontroller interface.

Transmitter: The transmitter encapsulates the transmit line frame generator, the line Time Division Multiplexer, the CRC generator, the PCM side control circuits, the transmission PCM frame counter, the VIDEO transmission buffer (FIFO) and AUDIO transmission buffer (FIFO) for rate adaptation, the transmission FIFO-control circuitry, the synchronising word generator and the transmission Protocol data shifters. The video and audio data are written to the transmitter FIFOs at a rate of 2.048 Mbits/sec under control of the PCM frame circuitry, and they are read at the Laser line rate of 2.304Mbits/sec under control of the laser frame circuitry. The audio and video streams are then multiplexed to the line frame, as well as the Protocol, sync-word and CRC data, and they are subsequently sent to the laser transceiver for final transmission to the Laser line. The CRC-4 associated polynomial has been selected for CRC generation and checking.

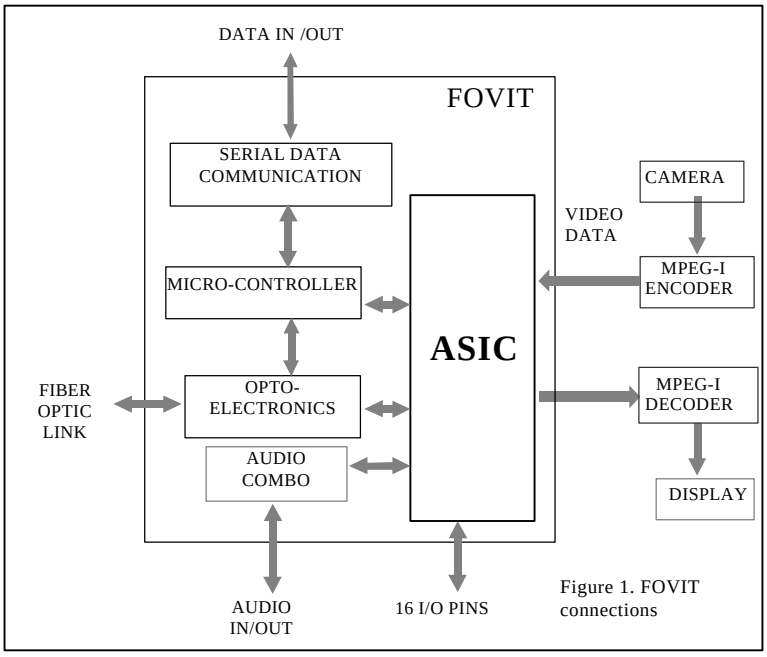


Figure 1. FOVIT connections

Receiver: The receiver encapsulates the laser receiver frame generator, the line demultiplexer, the CRC checker, the PCM side control circuits, the PCM receiver frame counter, the VIDEO receiver buffer (FIFO) and AUDIO receiver FIFO for rate adaptation, the receiver FIFO-control circuitry and the Receiver Protocol data shifters. The received laser data are written to the line RECEIVER_FIFOs at a rate of 2.304 Mbits/sec under control of the laser frame circuitry, and they are read at the rate of 2.048 Mbits/sec under control of the PCM frame circuitry. The Protocol data are extracted from the line and provided to the appropriate registers for further microcontroller access. CRC checking is also performed, for line quality monitoring. The above operations are validated upon receipt and detection of the correct sync word sequence.

Microcontroller Interface: The microcontroller interface is responsible for the control of the data transfer between the ASIC and the microcontroller. Á Chip select (CS), a read/write (RD/WR), 4 address and 8 bi-directional data signals are forming the interface, which is completely asynchronous as indicated by the absence of a clock. The rising edge of the CS signal validates the data, while the direction of flow is indicated by signal RD/WR. Ten register positions (Table 1.) form the register bank, and an interrupt line triggers the microcontroller each time a certain event has occurred (when the line is non-operational or the number of CRC error exceeds the CRC threshold). The detailed ASIC pin-out is shown at Table 2.

The main performance requirement is that the ASIC should be able to combine in the transmit direction the following:

a) 256 data bits from the 2,048Mbps serial data stream (compressed MPEG1 video with +/- 20ppm accuracy)

b) 8 data bits from PCM 64 Kbits/sec audio data stream from a National Semiconductor TP3057/67 CODEC/filter COMBO

c) 16 data bits from the microcontroller at 128 Kbits/sec.

The ASIC must be able also to de-multiplex the received data stream in the opposite direction. This implies the following frame structure:

FAW(Frame Alignment Word)	8
Video IF	256
Audio IF	8
microcontroller IF	16
CRC	4
FRAME WORD	288

Point to point transmission frame rate duration is set at 125ìsec. The duration of the bit is

$T = \frac{125\mu sec}{288} = 0.434\mu sec$, therefore

$f = \frac{1}{T} = 2.304\,\text{Mbits/sec}$

2. MICRO-CONTROLLER AND COMMUNICATION PORT

HARDWARE STRUCTURE

The architecture of the microcontroller is shown in Figure 3. The microcontroller uses an external ROM for storing its program and constants, and an external RAM for storing data. Each of the memories has a capacity of 32Kbytes. The connection to the communication port is implemented through a bi-directional voltage converter from TTL to RS-232 levels. The FOVIT-ASIC is connected as a normal memory component, and its internal registers are memory mapped. A Programmable Logic Device (PLD) performs the address decode on the board.

The RS232 serial communication and signalling between two FOVIT systems is done through the ASIC and the fiber link between them. The microcontroller writes its data to the ASIC internal registers, and then the ASIC is responsible to transmit these data through the fibre to the remote device. When data from the remote device arrive at the ASIC, the ASIC inform the microcontroller for the presence of new data through an interrupt. The microcontroller has direct access to the system functions for controlling the rest of the system through its 8-bit I/O port. These I/O control functions include Laser shutdown, power shutdown, laser power loss, etc.

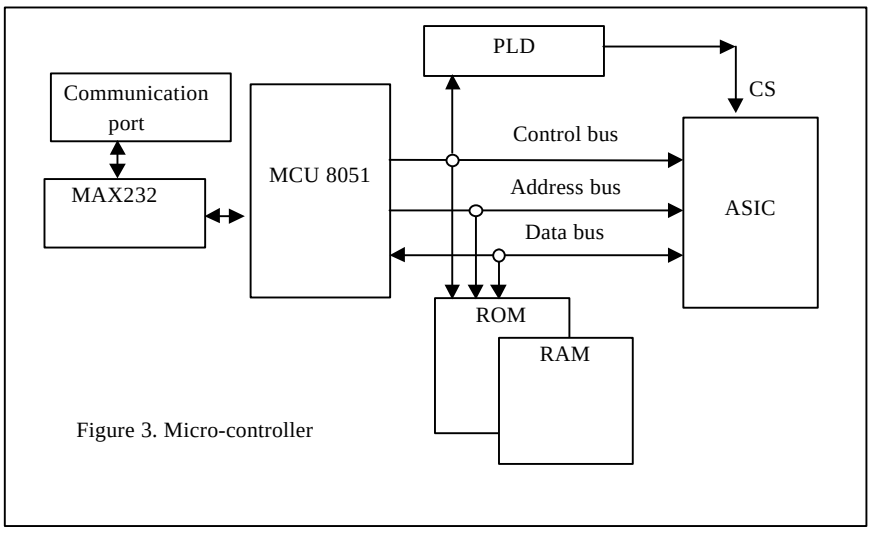


Figure 3. Micro-controller

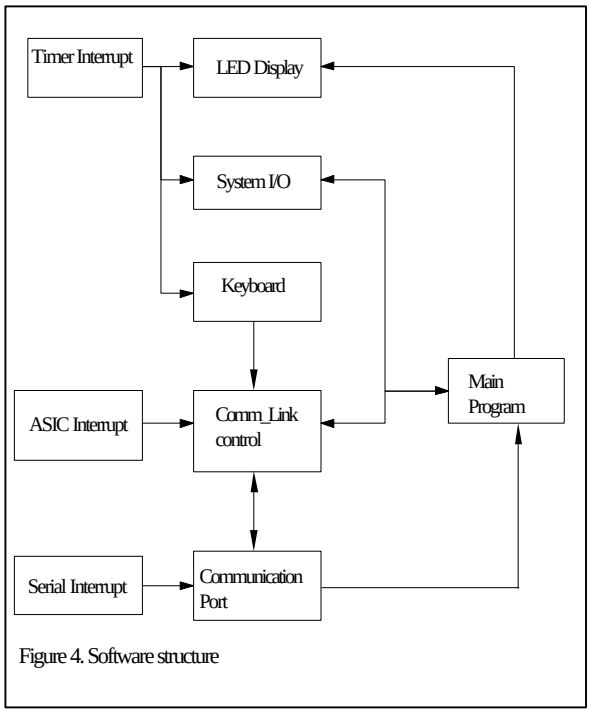


Figure 4. Software structure

The I/O port is not directly connected to the micro controller. The ASIC has some free I/O pins (totally 16 I/O) to be controlled by the microcontroller. The micro controller controls this I/O ports through the ASIC registers (Table 1). This section of the ASIC is completely irrelevant and independent from the communication link. Thus the keyboard and the LED display are controlled by the micro controller through the ASIC, which is used as an I/O extension of the micro controller.

SOFTWARE STRUCTURE

The software controls the system through its interrupt handlers. These handlers inform the main program (figure 4) of the system status or responds directly to the system. The main program is responsible for some operations and the handling of error conditions. Three interrupts are used for the control of the FOVIT. These are: 1) ASIC external interrupt, 2) Serial interface interrupt and 3) Timer interrupt.

1) ASIC external interrupt. This interrupt controls the ASIC for: a) Comm Link data from the remote

FOVIT unit, b) error conditions and c) the

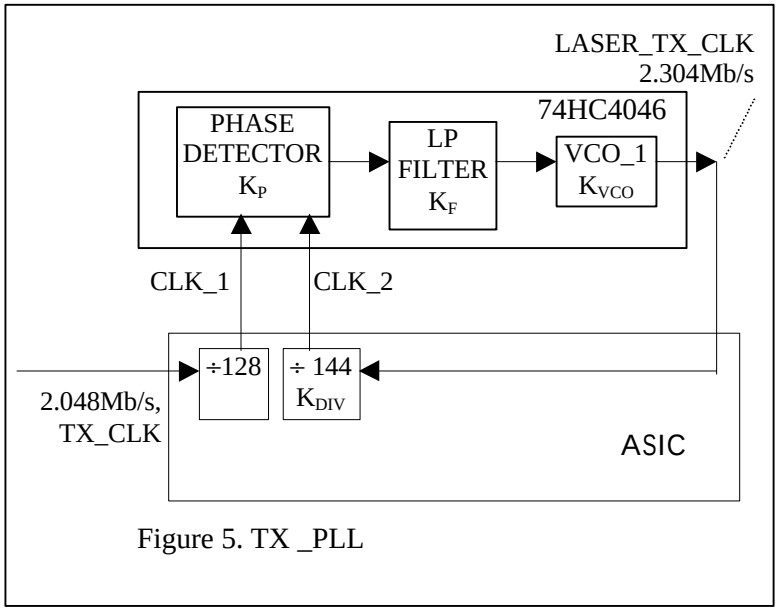


Figure 5. TX _PLL

general communication protocol between the units. If new data for serial communications are present from the remote unit then the handler transmits the serial data through the application layer of the serial transmission. If a command arrives from the remote unit the handler flags the main program to take action or responds by itself.

2) Serial interface interrupt. This interrupt performs the serial communication. When new data are to be transmitted to the remote unit, the handler sends the data to the Comm Link application routines for transmission.

3) Timer interrupt. The timer interrupt runs every 10msec and checks for time-outs, error conditions on the optical link, and the system input/output. The timer is also responsible for checking the keyboard, de-bouncing, and refreshing the LED display.

TRANSMITTER PLL

The transmitter PLL (Figure 5) converts the input clock TX_CLK from the video data 2.048MHz to the 2.304MHz, LASER_TX_CLK to produce the fiber optic line clock. The PLL chip is the 74HC4046 with external LP filter. The 74HC4046 contain a linear Voltage Controlled Oscillator (VCO), and three phase comparators.

The phase comparator II is used in the circuit and is an edge sensitive digital sequential network. This comparator is more susceptible to noise throwing the loop out of lock, but is less likely to lock onto harmonics. The VCO needs three external components, two resistors and one capacitor to set the frequency centre and the span (frequency range) f_{max} - f_{min}. The values are: f_{center}=2.300MHz, f_{max}= 2.500MHz and f_{min}=2.100MHz. The two dividers give the 16 KHz signals from subdivision of 2.048MHz transmission master clock (TX_CLK) and from the 2.304 line clock (LASER_TX_CLK). The loop was designed to generate a fixed multiple (X 144) of the input (16KHz) signal so it must have a low unity gain frequency (we choose f_2=2Hz). We put the frequency of the zero (the breakpoint of the low pass filter), f_1, at 0.5Hz.

The loop gain LG is given by

$$LG = K_P \cdot K_F \cdot \frac{K_{VCO}}{jw} \cdot K_{DIV} \qquad (1)$$

The low pass filter gain K_F (see figure 6) is given by

$$K_F = \frac{1 + jw \cdot R_{15} \cdot C_{18}}{1 + jw(R_{14} \cdot C_{18} + R_{15} \cdot C_{18})} \qquad (2)$$

The dividers are included in the ASIC to save

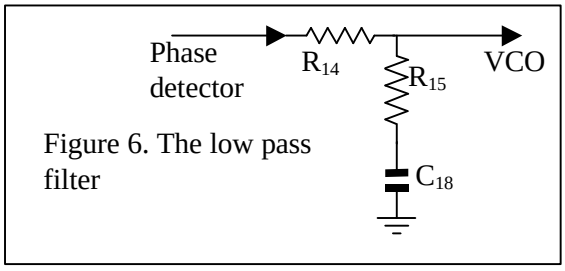


Figure 6. The low pass filter

board space.

The receiver PLL is very similar with the transmitter PLL and uses the same PLL IC and the same dividers. The receiver PLL converts the received line clock (LASER_RX_CLK) at 2.304 Mbits/sec, from the clock recovery circuitry down to generate the 2.048 Mbits/sec RX_CLK clock signal.

OPTO-ELECTRONICS

The opto-electronics was designed to provide the communication media of the system. In this part of the system the three different signals after they have been combined together at the ASIC change from electronic phase to optical (light) phase and vice-versa. The system is suitable to accommodate a variety of opto-electronic transmitters and receivers pairs, with minor alternations every time, ranging from LEDs to LASERs and for a variety of fiber optic media ranging from multi-mode to single mode type fibers. The PIN Receiver/Amplifier LH0082 (see figure 7.) is a low noise, fiber optic receiver and includes a wide-bandwidth FET-input amplifier, a 2.4Volt reference voltage and a comparator with hysteresis to convert the analog received signal to a TTL/CMOS compatible logic signal. The **TRU050** clock recovery PLL is a crystal stabilised, phase-locked-loop that extracts the clock signal from the received digital data stream and regenerates the data. It is capable to recover any data patterns reducing the need for a data line encoding. Input data should originate in a device with a crystal stabilised clock source and be in an NRZ format at TTL/CMOS levels. The

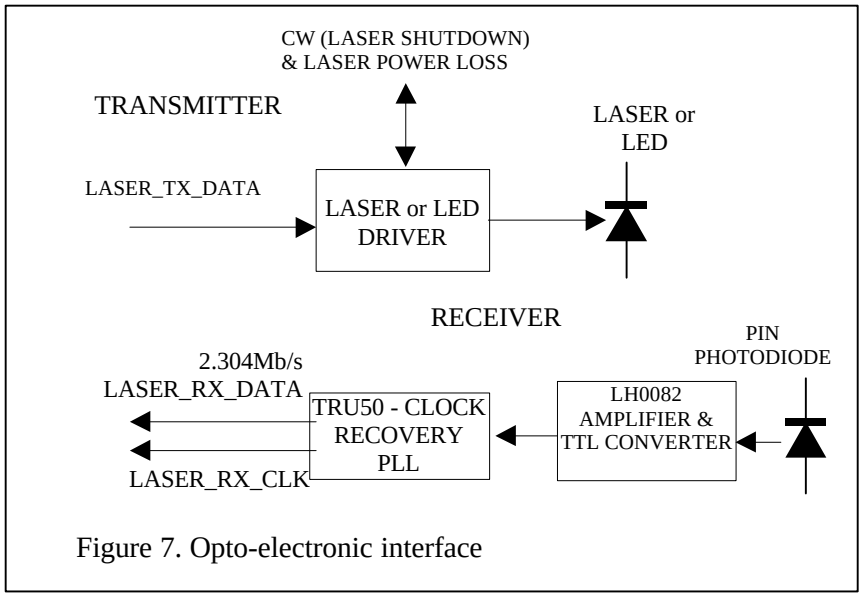


Figure 7. Opto-electronic interface

TRU050 contains a phase detector an operational amplifier and voltage controlled crystal oscillator at 2.304MHz. It only requires an external low pass filter.

VOICE SIGNAL ENCODER/DECODER

The audio encoder/decoder is the National Semiconductor serial interface TP3057 or TP3067 A-law CODEC/Filter COMBO. TP3057/67 includes the necessary ADC, DAC, preamplifier, filters, parallel to serial converters and the serial PCM interface. More detailed, the encode portion consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering band-pass filter from 200Hz to 3400Hz. Also are included the auto zero circuitry and an A-law companding encoder. The decode portion consists of an expanding decoder, a low-pass filter and a power amplifier. The IC requires two 2.048MHz, transmit and receive master clocks which may be asynchronous, transmit and receive bit clocks which are the same with transmit and receive master clocks (Figure 2). It also requires from the ASIC transmit and receive frame sync

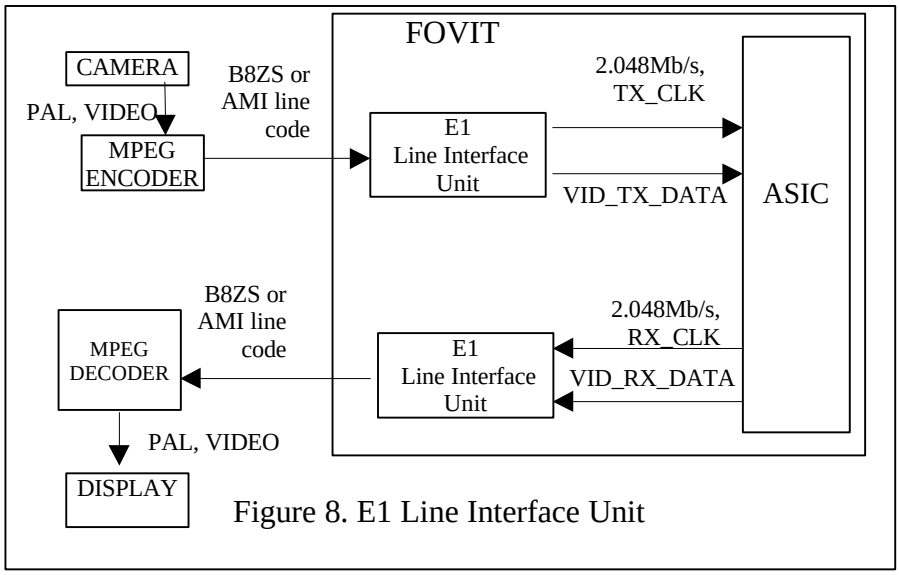


Figure 8. E1 Line Interface Unit

pulses in order to send or receive the voice data bits at the right time slot during the frame construction.

MPEG ENCODER/DECODER E1 INTERFACE

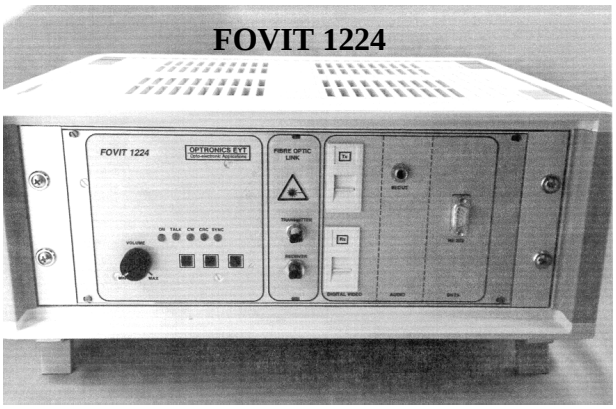
The E1 Board combines the complete analog transmit and receive interface between the encoded video data line and the ASIC. It can be easily controlled by a microcontroller. It uses the CS61304 chip from Crystal Semiconductor witch provides Line Driver, Jitter attenuator and clock recovery functions. At this point a user can insert a compressed video signal (MPEG1 of 2.048Mbps) or any other data at 2.048 Mbits/sec to carry it on the other side of a link. The same E1 module operates also inversely, that is, video and data received from the other side are provided in a standard format of 2.048Mbps to be directed to an MPEG1 receiver - decoder. The E1 Line Interface Unit (LIU) converts the B8ZS or AMI encoded signal to TTL/CMOS logic levels and extract from the serial data stream the 2.048MHz clock.

DISCUSSION

The FOVIT system has been implemented with the following configuration:

1. 1300nm LED at –10dBm optical transmitter
2. pin-photodiode with –35dBm sensitivity
3. 2km of multi-mode optical fiber (62.5/125)

Successfully operation has been verified and full duplex data, voice and video transmission performed through the multi-mode optical fiber. The system allows in campus or inter building hands free tele and video conferencing.



ACKNOWLEDGEMENT

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TABLE 1. REGISTER MAP OF THE ASIC

NAME	ADDRESS	
STATUS REGISTER	00	The MICROCONTROLLER can read these bits to know the general operation of the device and the situation of the link
COMMAND REGISTER	00	The MICROCONTROLLER can write to these bits to reset the ASIC
INTERRUPT SOURCE REGISTER	01	The MICROCONTROLLER reads this register to determine the source of interrupt
INTERRUPT MASK REGISTER	01	The MICROCONTROLLER can disable the source of one interrupt by setting the corresponding bit
CRC ERROR REGISTER	02, 03	16 bit counter for bit error measurements
CRC RESET CYCLE, ADDRESS	02, 03	16 bit counter for bit error measurements
DATA DIRECTION CONTROL REGISTER A & B	05, 06	Two registers to control the direction of the MPU controllable general purpose I/O pins of the ASIC
DATA INPUT/OUTPUT REGISTER A & B	07, 08	Two Registers to control the logic state of the MPU controllable general purpose I/O pins
TRANSMIT & RECEIVE PROTOCOL REGISTER LOW & HIGH	09, 0A	Control, communications and Serial Port RS232 support

TABLE 2. ASIC PIN - OUT DESCRIPTION

pin_name	description	I/O	# PINS
RESET	Asynchronous reset. Input active low. It is used for chip initialisation on power-up	I	1
CS	Chip select input, active low. Enables data transfer (read / write) from / to the chip. The microcontroller interface is asynchronous, and the data are written / read in relation to the rising edge of CS	I	1
RW	Read / Write control input signal. When high (logic '1'), read operation is selected. When low (logic '0') a write is performed	I/O	1
ADDR (3: 0)	Address bus. Four input signals are needed in order to select one of the 10 internal registers of the IC	I	1
DATA(7..0)	Bi-directional data bus. Allow for data transfer between the microcontroller and the ASIC	I/O	1
IRQ	Interrupt Request. Open drain output, active low. It is activated on one of the following reasons: (a) when Loss of Frame Alignment (LFA) occurs, i.e. when the line is non-operational, (b) when the number of detected CRC errors exceeds the CRC threshold, (c) when Protocol data have been received at the receiver side, (d) when Frame Alignment sync is recovered (SYNC) after a sync loss. It is clarified that these interrupt sources can be individually masked on programmer's choice	O	1
TX_CLK2	Audio / Video side transmitter clock input. A 2.048Mbits/sec clock provided by the video module, controlling the transfer of both video and audio data to the optical line side	I	1
VID_TX_DATA	Video data stream input form the Video module, 2.048Mbits/sec rate	I	1
AUD_TX_DATA	Audio data stream input from the Audio module, 64Kbits/sec rate at 2.048Mbits/sec bursts	I	1
RX_CLK2	Audio / Video side receiver clock output. A 2.048Mbits/sec clock provided by the ASIC, controlling the transfer of both video and audio data from the optical line side. This clock is phase4ocked to the RX_ICLK (laser side).	O	1
VID_RX_DATA	Video data stream output to the Video module, 2048Mbits/sec rate	O	1
AUD_RX_DATA	Audio data stream output to the Audio module, 64Kbits/sec rate at 2.048Mbits/sec bursts.	O	1
TX_ICLK	Laser transmit interface clock output. A 2.304Mbits/sec clock provided from the ASIC, controlling the transmission of both video and audio data through the optical line. This clock is phase-locked to the TX_CLK2	O	1
LAS_TDATA	Laser side data stream output to the laser transceiver, 2304Mbits/sec rate	O	1
RX_ICLK	Laser receive interface clock input. A 2.304Mbits/sec clock provided to the ASIC by the clock recovery circuit, controlling the reception of both video and audio data from the optical line	I	1
LAS_RDATA	Laser side data stream input from the laser transceiver, 2304Mbits/sec rate	I	1
FSX	Frame Sync Transmit. A PCM frame sync pulse output provided to the Audio combo device for Tx voice data alignment	O	1
FSR	Frame Sync Receive. A PCM frame sync pulse output provided to the Audio combo device for Rx voice data alignment	O	1
IODATA(I5:0)	16 i/o general purpose bidirectional ports	I/O	1
CLK_1	clock output connected to control the external TX_PLL. It is 16KHz control clock signal from subdivision of TX_CLK2	O	1
CLK_2	clock output feedback connected to phase detector of TX_PLL to control the frequency of the external TX_PLL.	O	1
CLK_3	clock output connected to control the external RX_PLL	O	1
CLK_4	clock output connected to control the external RX_PLL. It is 16KHz control clock signal from subdivision of RX_CLK2	O	1

Fourteen (14) power pins (Vdd and Vss) have been used, according to the ASIC vendor's recommendations. Summarising, the ASIC contains 12 input signals, 9 output signals and 16 bi-directional signals, as well as 5 test and 14 power pins.

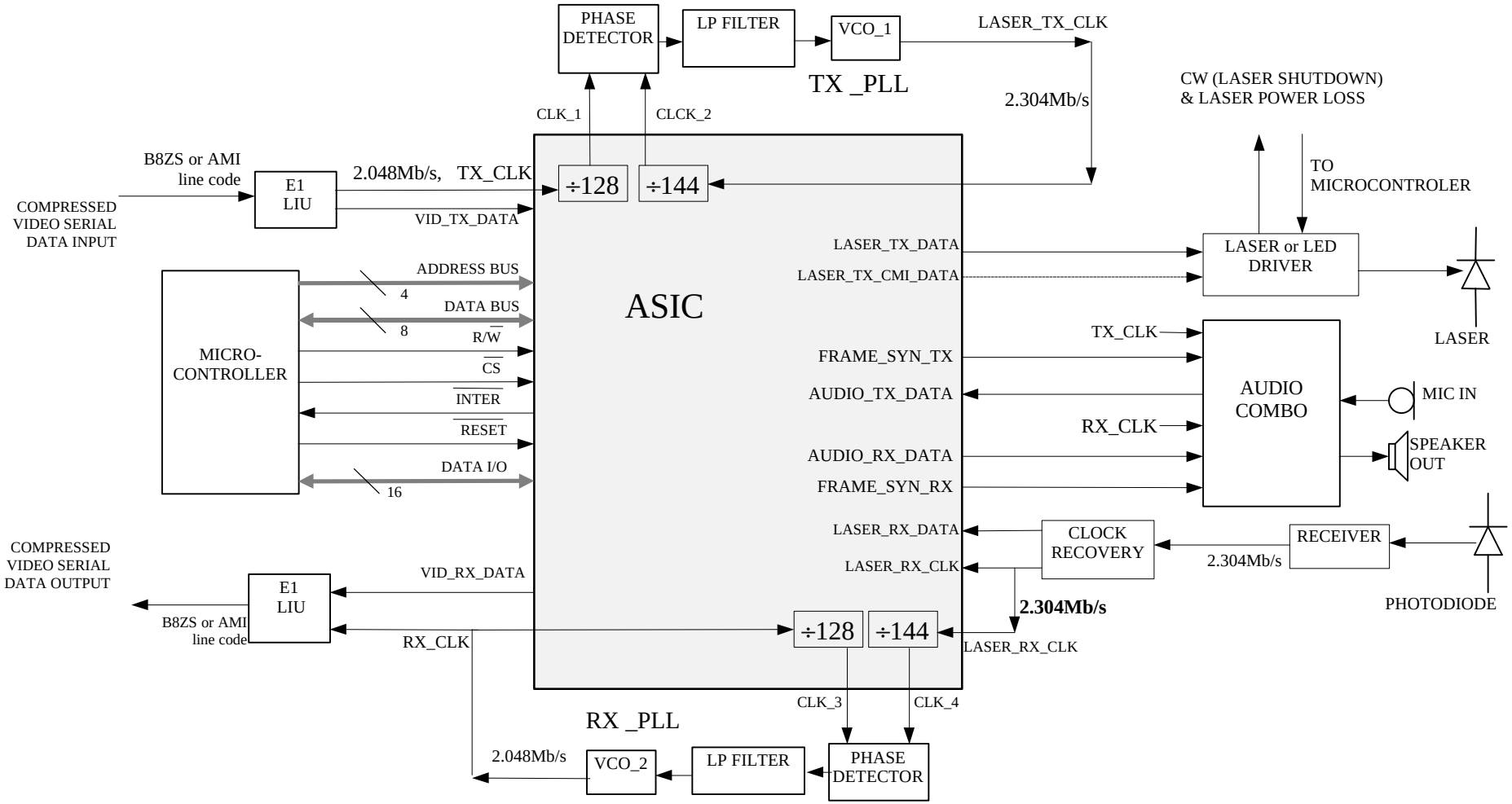
PHASE DETECTOR
LP FILTER
VCO_1
LASER_TX_CLK
TX _PLL
2.304Mb/s
CW (LASER SHUTDOWN)
& LASER POWER LOSS
CLK_1
CLCK_2
B8ZS or AMI line code
E1 LIU
2.048Mb/s, TX_CLK
÷128
÷144
TO MICROCONTROLER
COMPRESSED VIDEO SERIAL DATA INPUT
VID_TX_DATA
LASER_TX_DATA
LASER_TX_CMI_DATA
LASER or LED DRIVER
LASER
ADDRESS BUS
4
DATA BUS
8
R/W
CS
INTER
RESET
DATA I/O
16
MICRO-CONTROLLER
ASIC
TX_CLK
FRAME_SYN_TX
AUDIO_TX_DATA
RX_CLK
AUDIO_RX_DATA
FRAME_SYN_RX
AUDIO COMBO
MIC IN
SPEAKER OUT
LASER_RX_DATA
LASER_RX_CLK
CLOCK RECOVERY
RECEIVER
2.304Mb/s
PHOTODIODE
COMPRESSED VIDEO SERIAL DATA OUTPUT
VID_RX_DATA
E1 LIU
B8ZS or AMI line code
RX_CLK
2.304Mb/s
LASER_RX_CLK
÷128
÷144
CLK_3
CLK_4
RX _PLL
2.048Mb/s
VCO_2
LP FILTER
PHASE DETECTOR

Figure 2.