

## Electrical Behavior of SOI-Like Structures Formed under High Pressure in Nitrogen or Oxygen Implanted Silicon

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Separation of silicon layer from substrate by oxygen or nitrogen implantation is one of the main ways in the development of silicon-on-insulator (SOI) materials. Implantation of oxygen is now well-established and widely used technology of the SOI wafer creation. Due to some unsolved problems (e.g. crystallization of the nitride layer, large leakage current and non-uniform Si/Si<sub>3</sub>N<sub>4</sub> interface) the nitrogen implantation does not found wide application in modern electronics. To benefit both from the advantages of silicon nitride (a diffusion inhibition and impurity gettering) and of silicon dioxide (a low leakage current and a planar interface top Si layer / buried oxide) and for the development of the radiation hard materials, co-implantation of oxygen and nitrogen is developing for the fabrication of SOI material with combined insulator.

Completed removal of the radiation-induced defects is the main problem of all implantation based technologies, which is enhanced in these cases due to the high fluences used. An application of the high pressure during high temperature post-implantation annealing is a promising way to manage the problem by the transformation of the radiation defects. Electrical and structural properties of multilayer structures formed in silicon implanted with high fluence of either nitrogen or oxygen ions and treated under enhanced hydrostatic pressure of argon ambient up to 1.4 GPa at temperatures ranged 800 – 1300°C has been studied in the present work. Based on current-voltage, capacitance-voltage, cross-sectional transmission electron microscopy, and secondary ion mass spectroscopy measurements, it has been found that the application of HP during post-implantation anneals, allows one to change the defect distribution between the insulator layer and the silicon, and to achieve a

degree of control on the charges at interfaces and the carrier concentration in the top silicon layer.